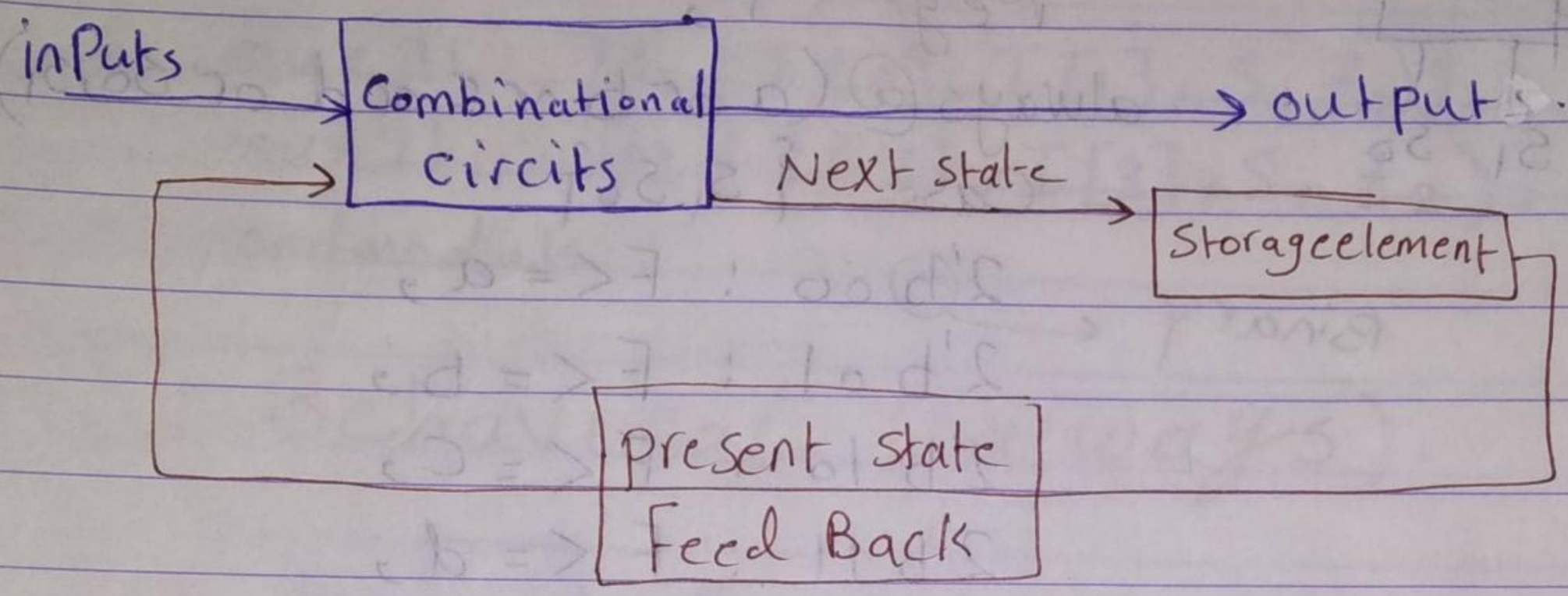
Chapter 5

متزامن Synchronous Sequential Circits.

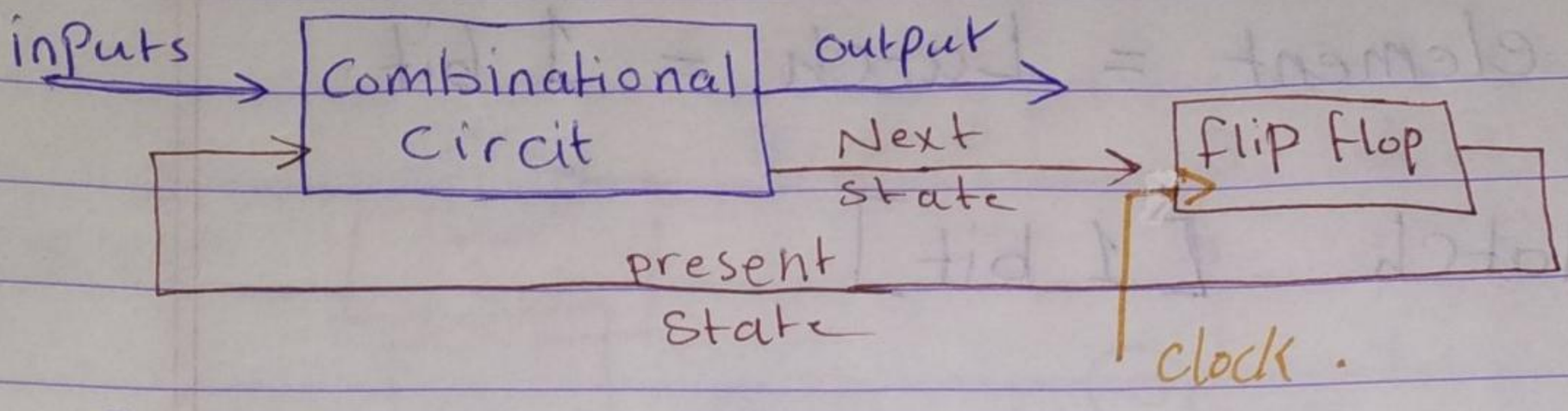


* outputs depends on inputs and previous outputs.

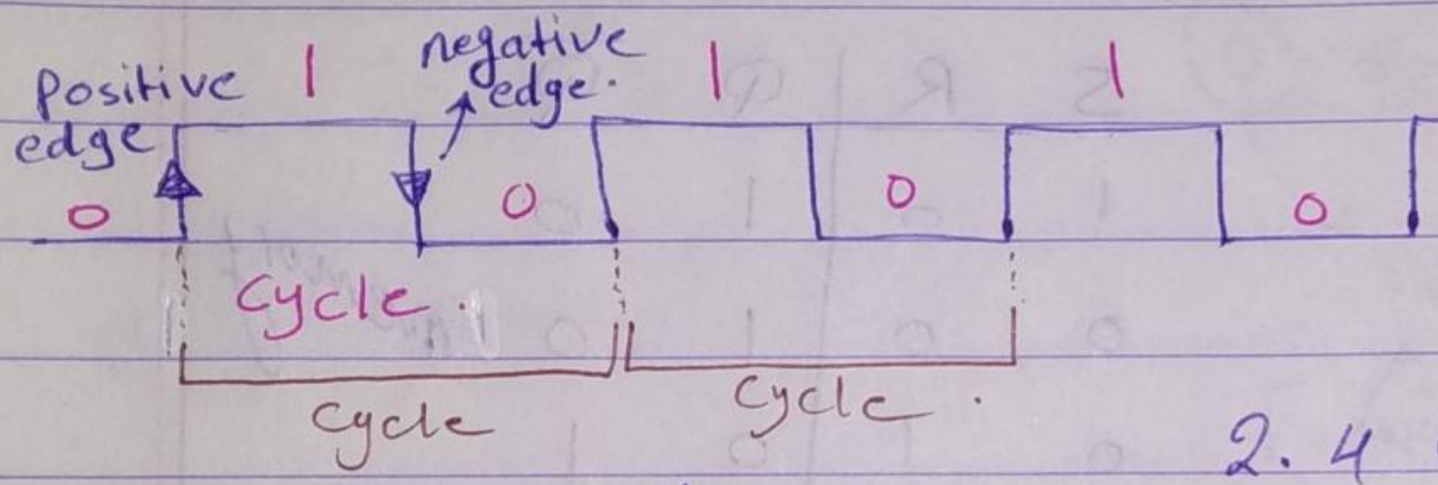
Electrical circits.

- Analog circit
- Digital circit.
  - Ch4 Combinational circits.
  - Sequential circits
    - Ch5 متزامن synchronous clocks.
    - غير متزامن Asynchronous clocks

* Synchronous Sequential circuit :—



Flip flop = memory 1 bit.

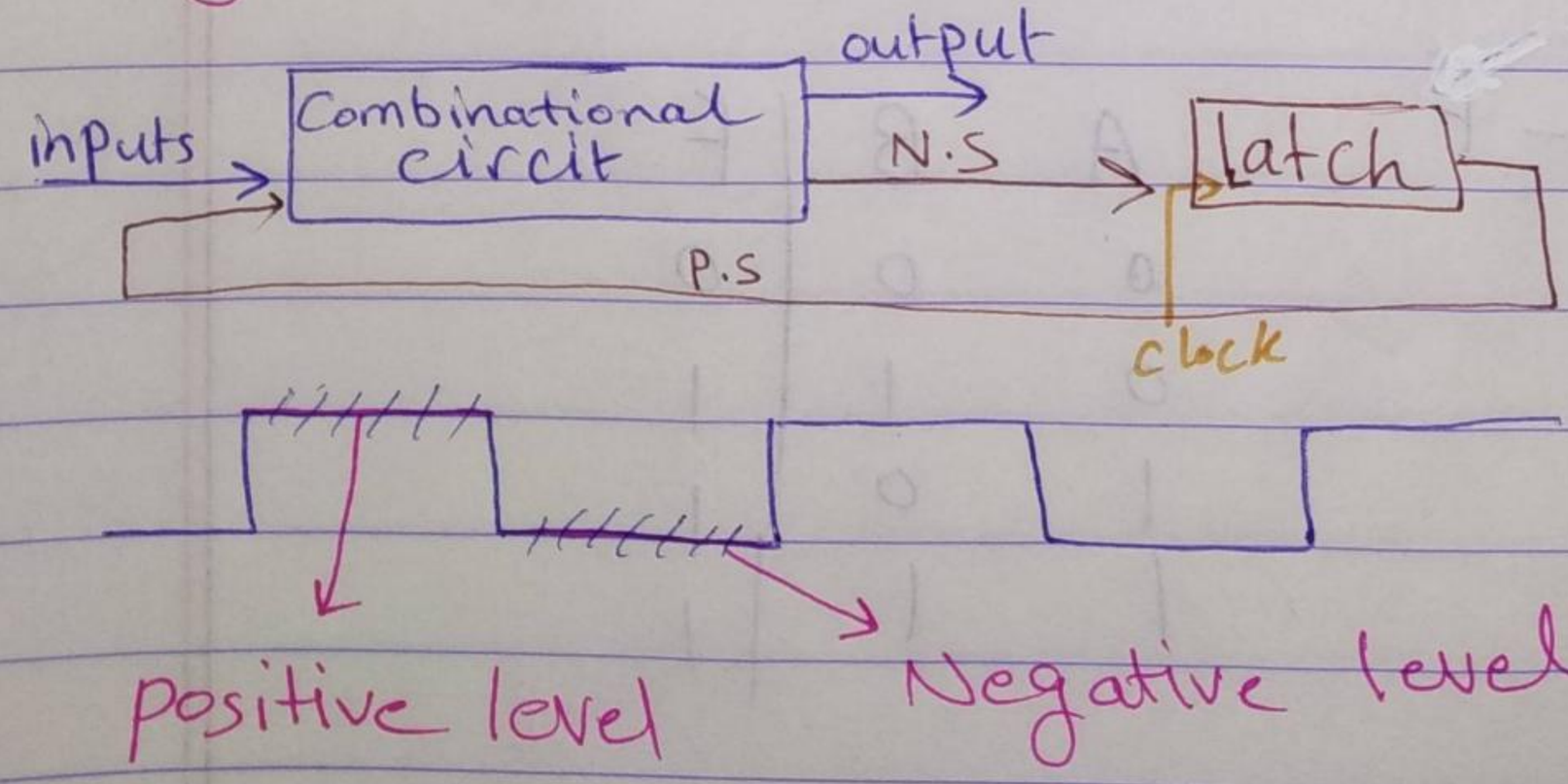


$2.4\ GHz = 2.4 \times 10^9\ \frac{1}{s}$.

$$\text{Frequency} = \frac{1}{\text{Time}}$$

* positive edge :- 1 ← 0 ہو
* Negative edge :- 0 ← 1 ہو

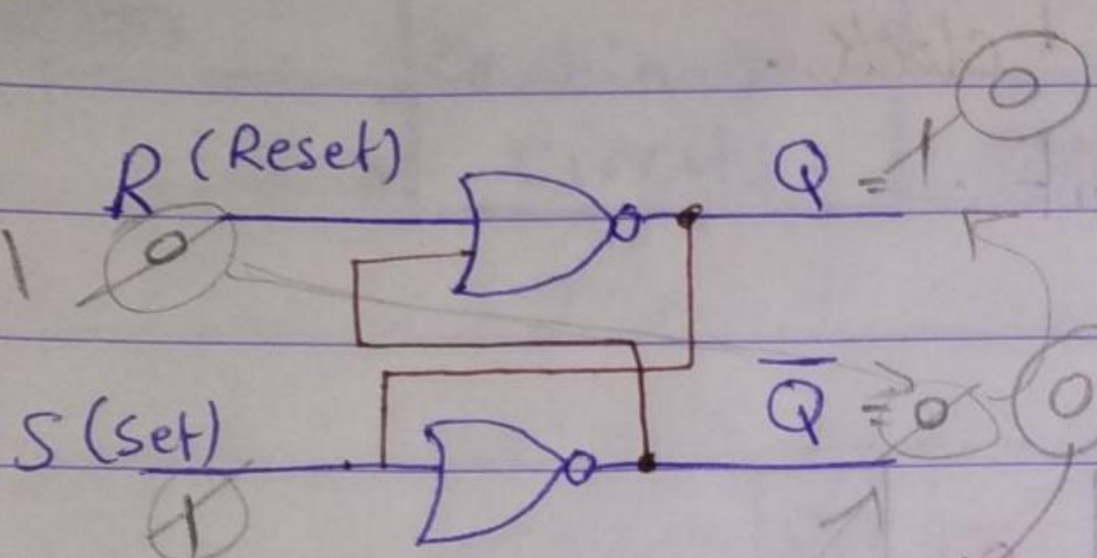
* Asynchronous Circits :—



* Asynchronous Circuit :-

memory element = Latch = 1 bit.

① SR - latch [1 bit]:



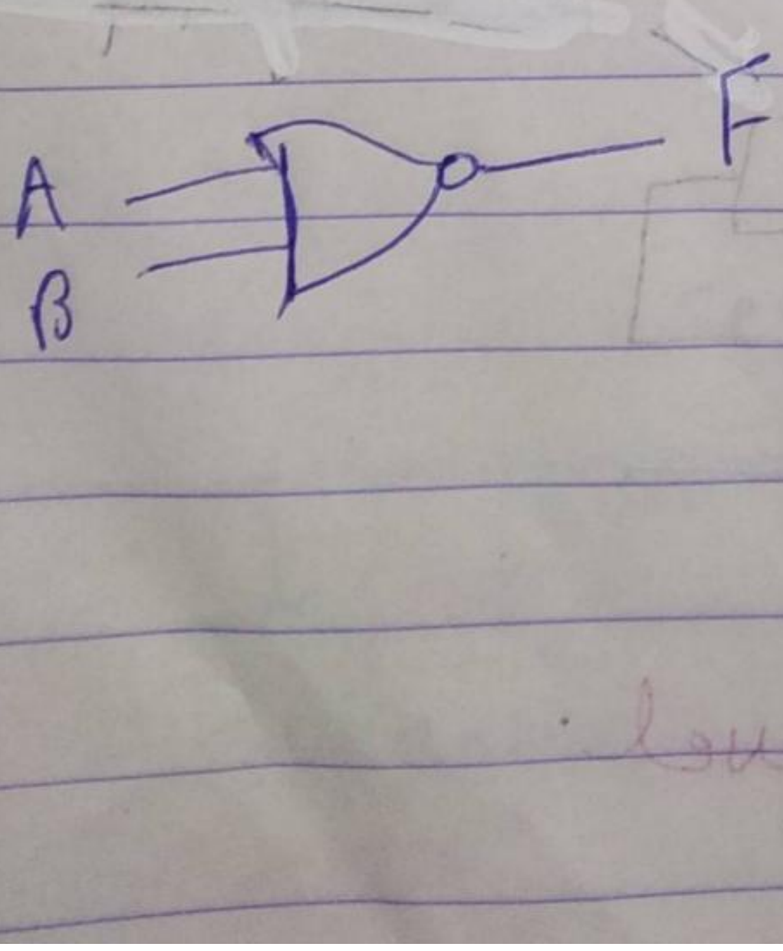
feed back → P.S

S	R	Q	$\overline{Q}$	
1	0	1	0	
0	0	1	0	memory.
0	1	0	1	
0	0	0	1	memory.
1	1	0	0	[forbidden].

[forbidden] ممنوع يطلع نفس لوضع

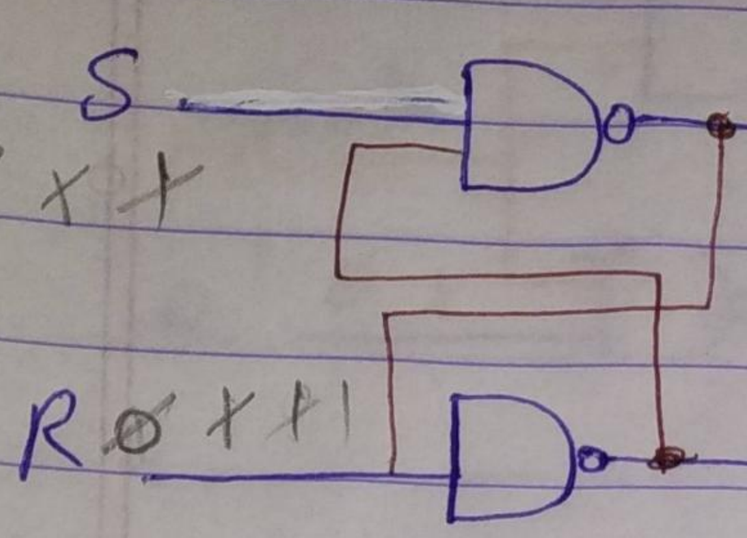
✓ Function Table

✗ truth table ولَيس

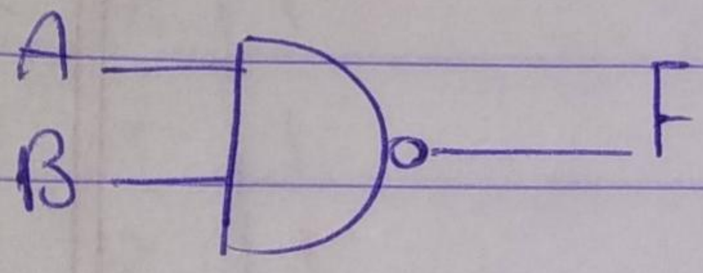


A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

② SR-Latch with NAND gate.



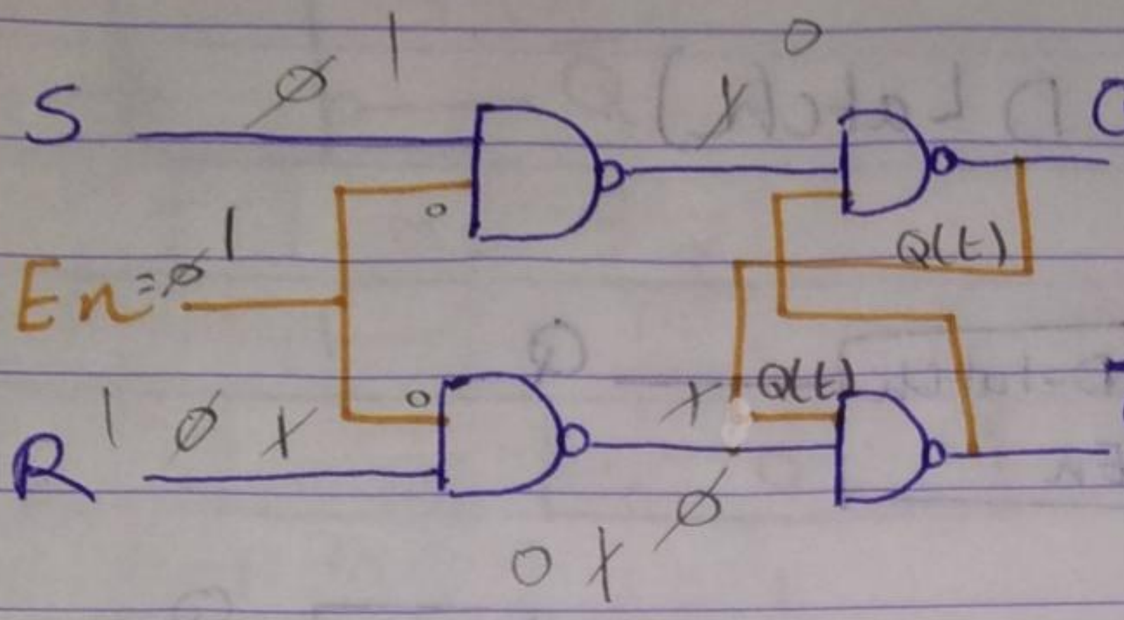
S	R	Q	$\overline{Q}$	
1	0	1	0	
1	1	a	$\overline{a}$	memory
0	1	0	1	
1	1	1	0	memory
0	0	1	1	[forbidden]



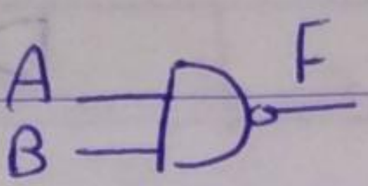
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

Function Table.

③ SR Latch with enable



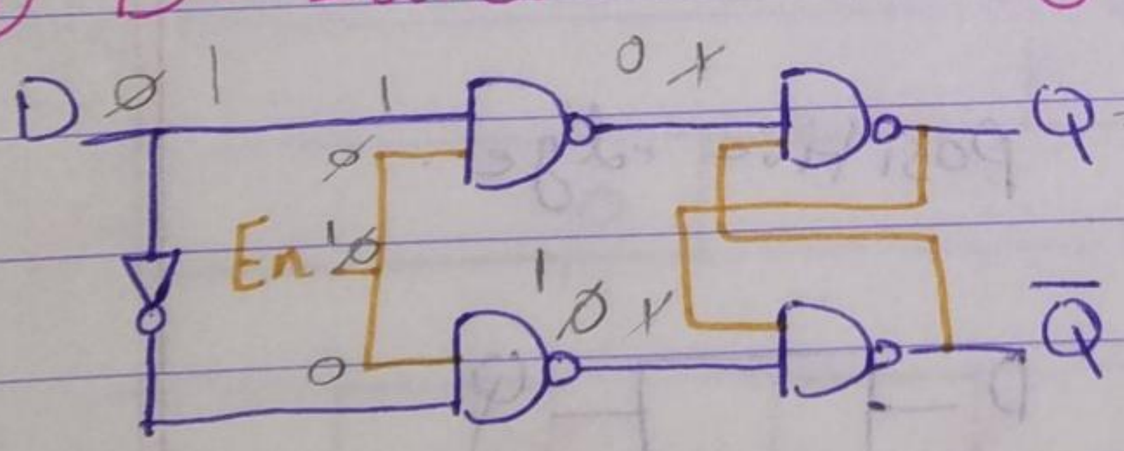
NAND gate



A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

En	S	R	memory.
0	X	X	No change → Q(t+1) = Q(t).
1	0	0	No change → Q(t+1) = Q(t).
1	0	1	Q[t+1] = 0.
1	1	0	Q(t+1) = 1.
1	1	1	Forbidden.

④ D-Latch - memory element Asynchronous



En	D	
0	X	No change (Q(t+1) = Q(t).
1	0	Q(t+1) = 0
1	1	Q(t+1) = 1

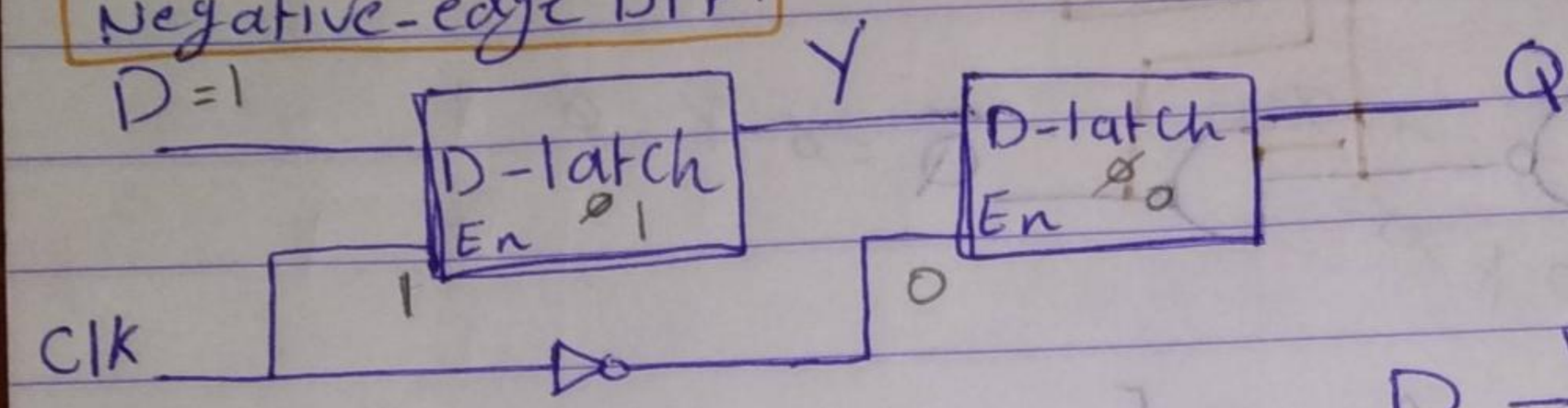
[فش forbidden لأنه input واحد.] أهميته.

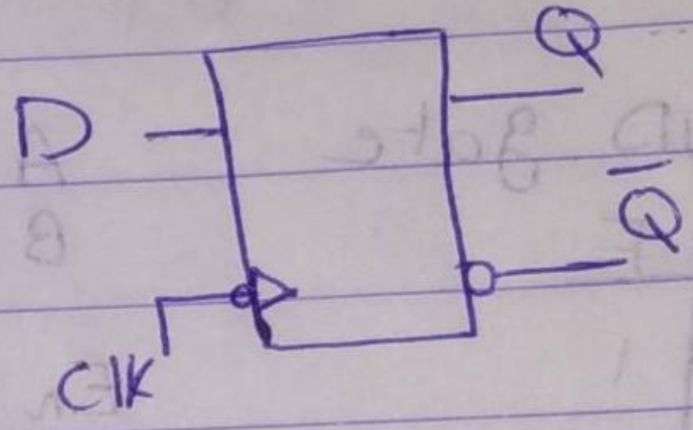
① DFF

Edge - Triggered D - Flip Flop.

(Two Latches - D Latch).

Negative-edge DFF.





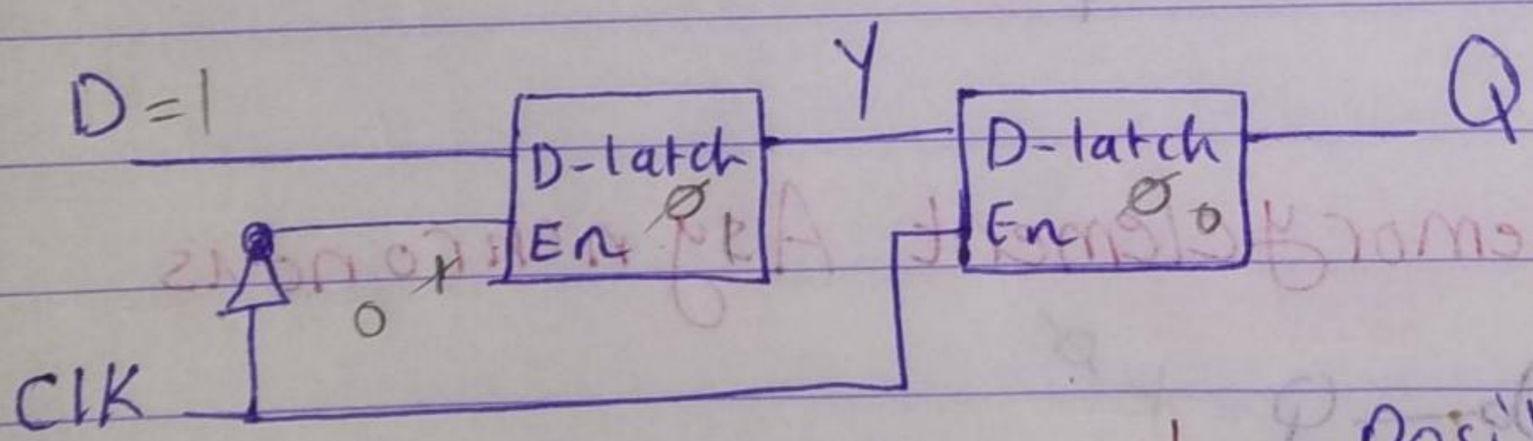
if - Clk = 1

1

↓ 0 (negative edge).

$Q(t+1) = D$ ↵

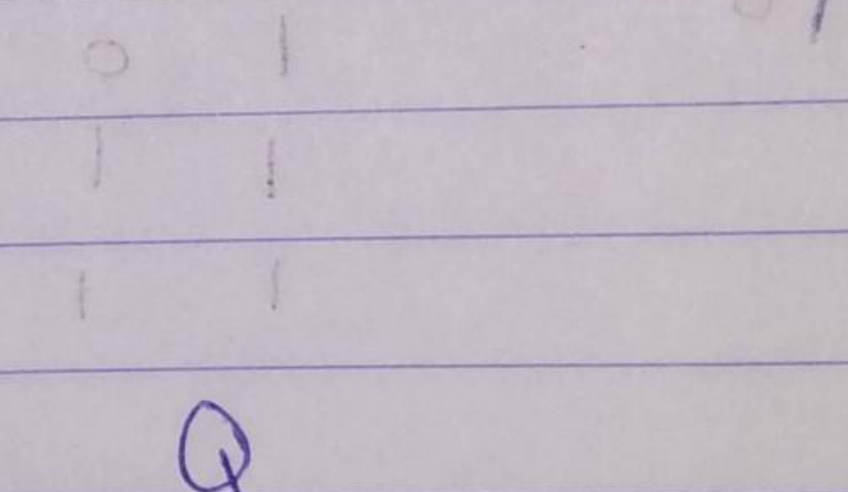
positive-edge DFF.



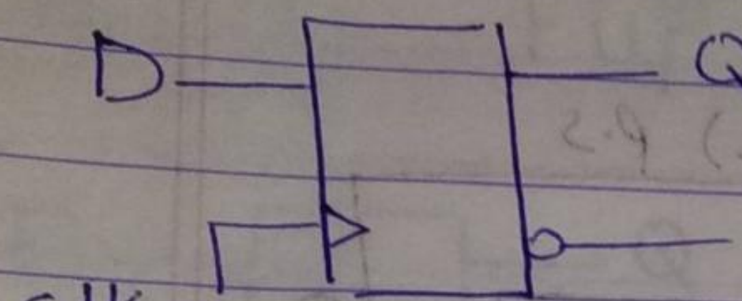
1 positive edge.

Clk = 0 ↑ 0

$Q(t+1) = D$

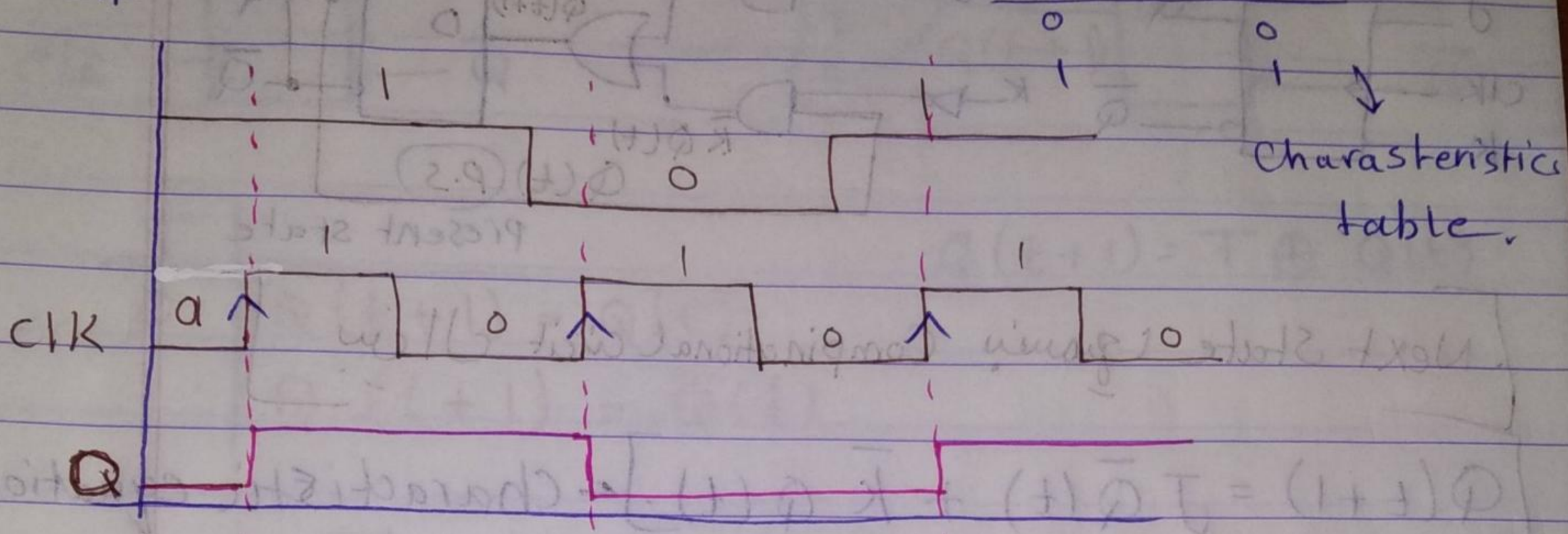


Positive edge.



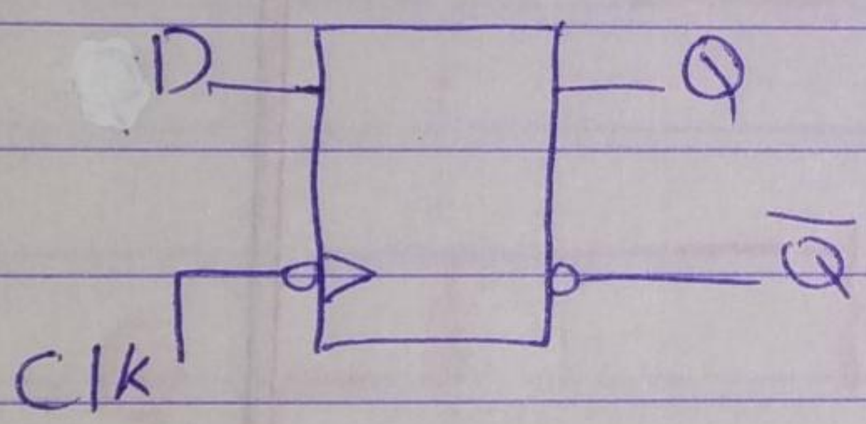
D	Q(t+1)
0	0
1	1

↓
Charasteristics table.

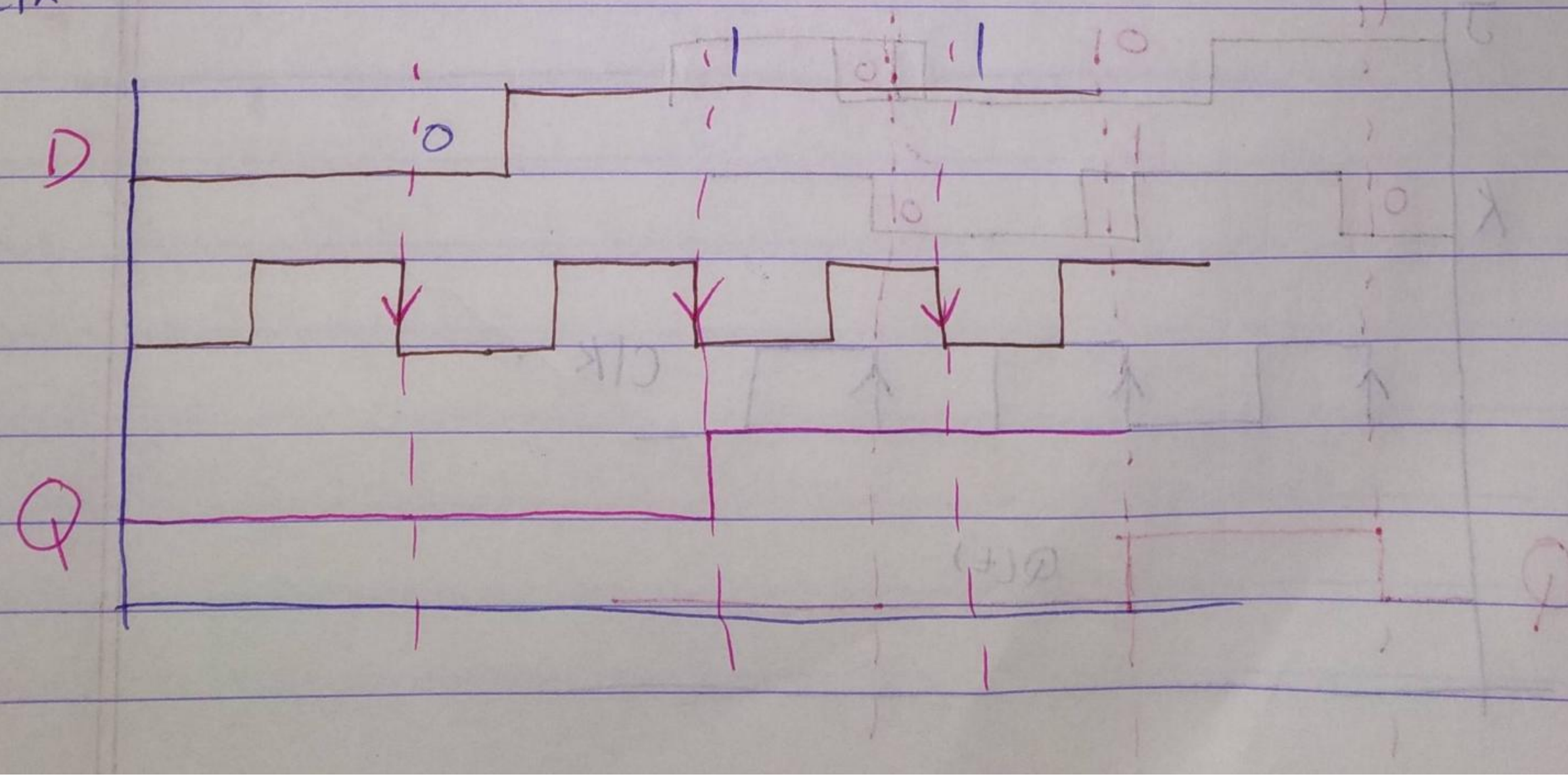


Timing Diagram-

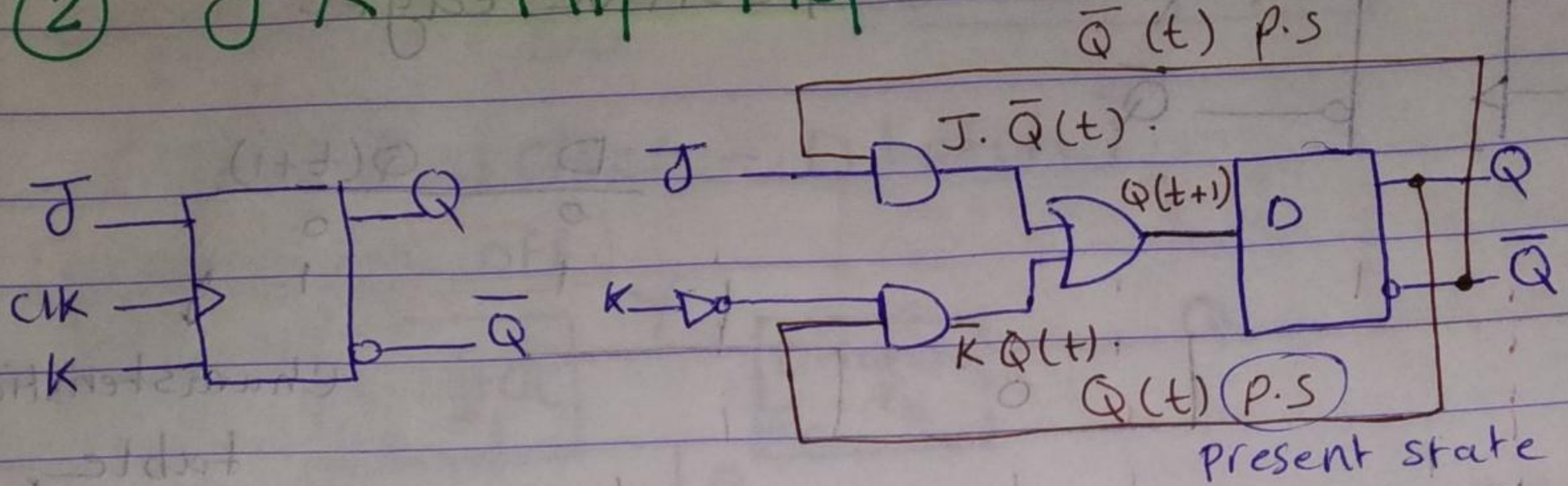
Negative edge.



$Q(t+1) = D$



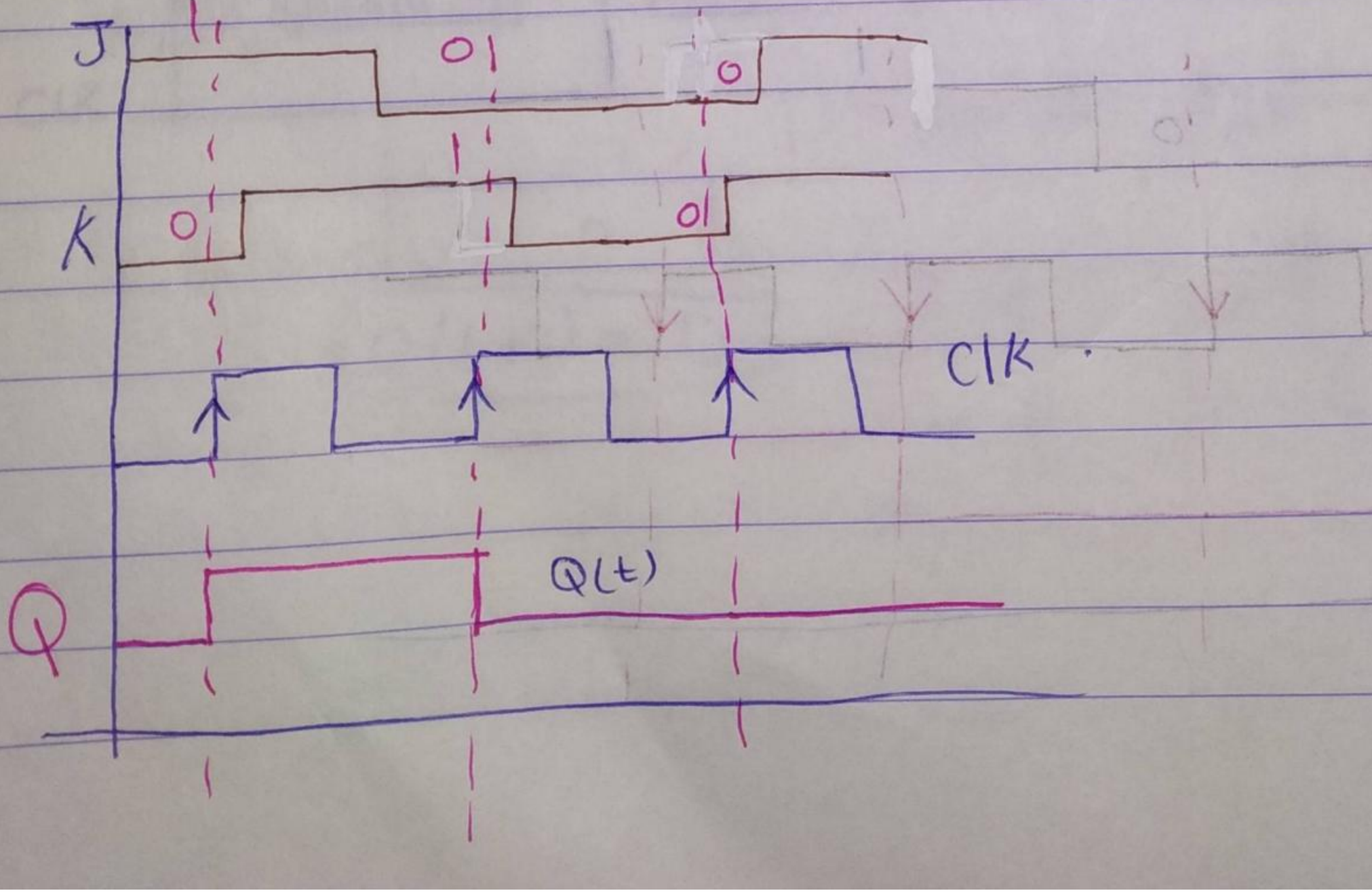
② JK Flip Flop.



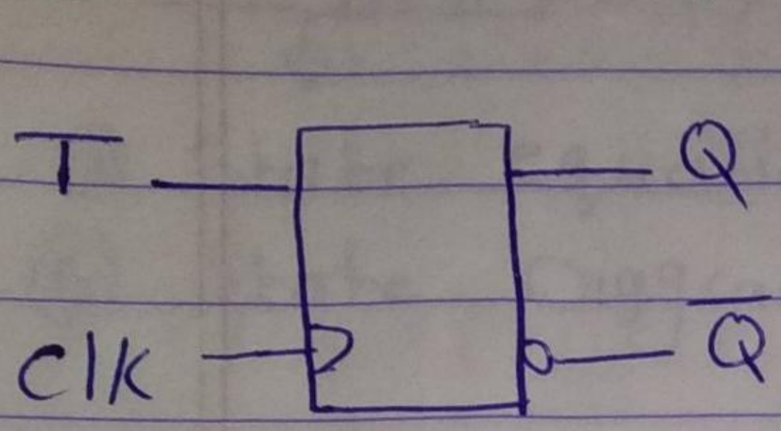
[Next State يسمى Compinational circit بـ ال]

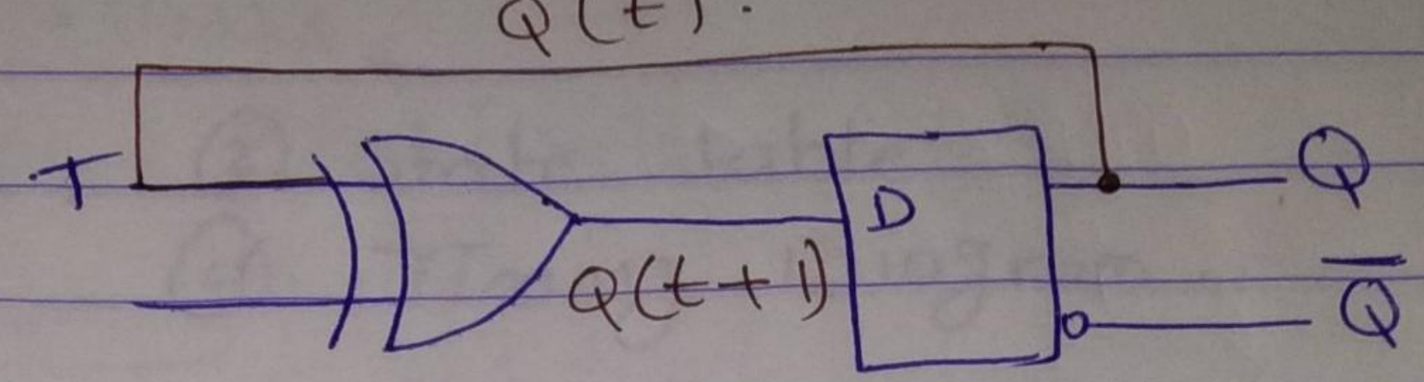
[$Q(t+1) = J\bar{Q}(t) + \bar{K}Q(t)$] ← Characteristic equation.

J	K	
0	0	$Q(t+1) = Q(t)$ ← (No change).
0	1	$Q(t+1) = 0$
1	0	$Q(t+1) = 1$
1	1	$Q(t+1) = \bar{Q}(t)$.



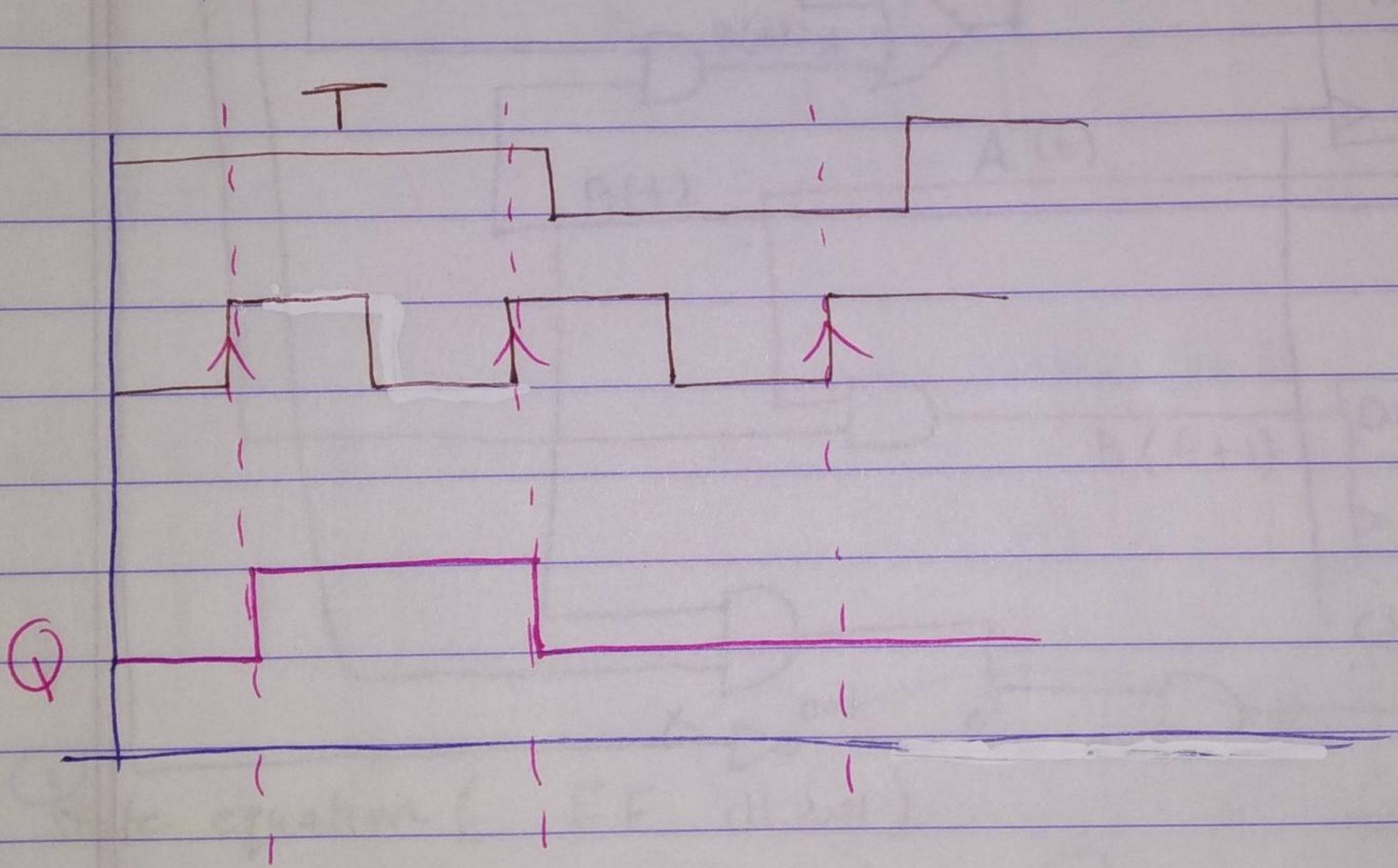
(3) T Flip Flop.





T	
0	$Q(t+1) = Q(t)$.
1	$Q(t+1) = \overline{Q}(t)$

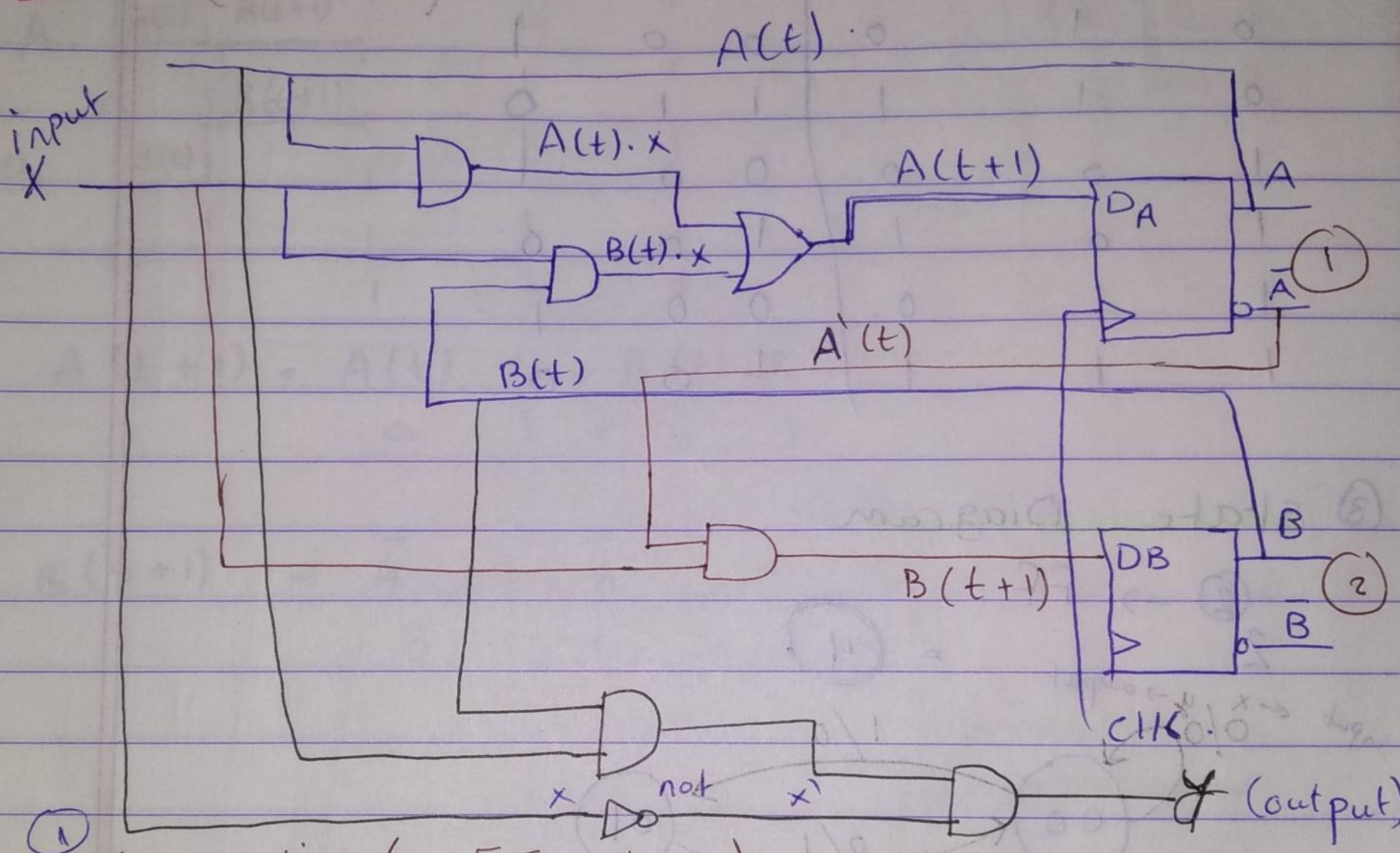
$Q(t+1) = T \oplus Q(t)$.



Analysis For clocked sequential circuit.

① State equation, ② State table.
③ State Diagram. ④ Timing Diagram.

ex



State equation (FF بعدد ال).

① $A(t+1) = A(t).x + B(t).x$ ——— ①

② $B(t+1) = \bar{A}(t).x$

$y = [A(t) + B(t)].x'$ [P.S + input].

② State table :

$A(t+1) = A(t).X + B(t).X$

P.S		input	N.S		output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

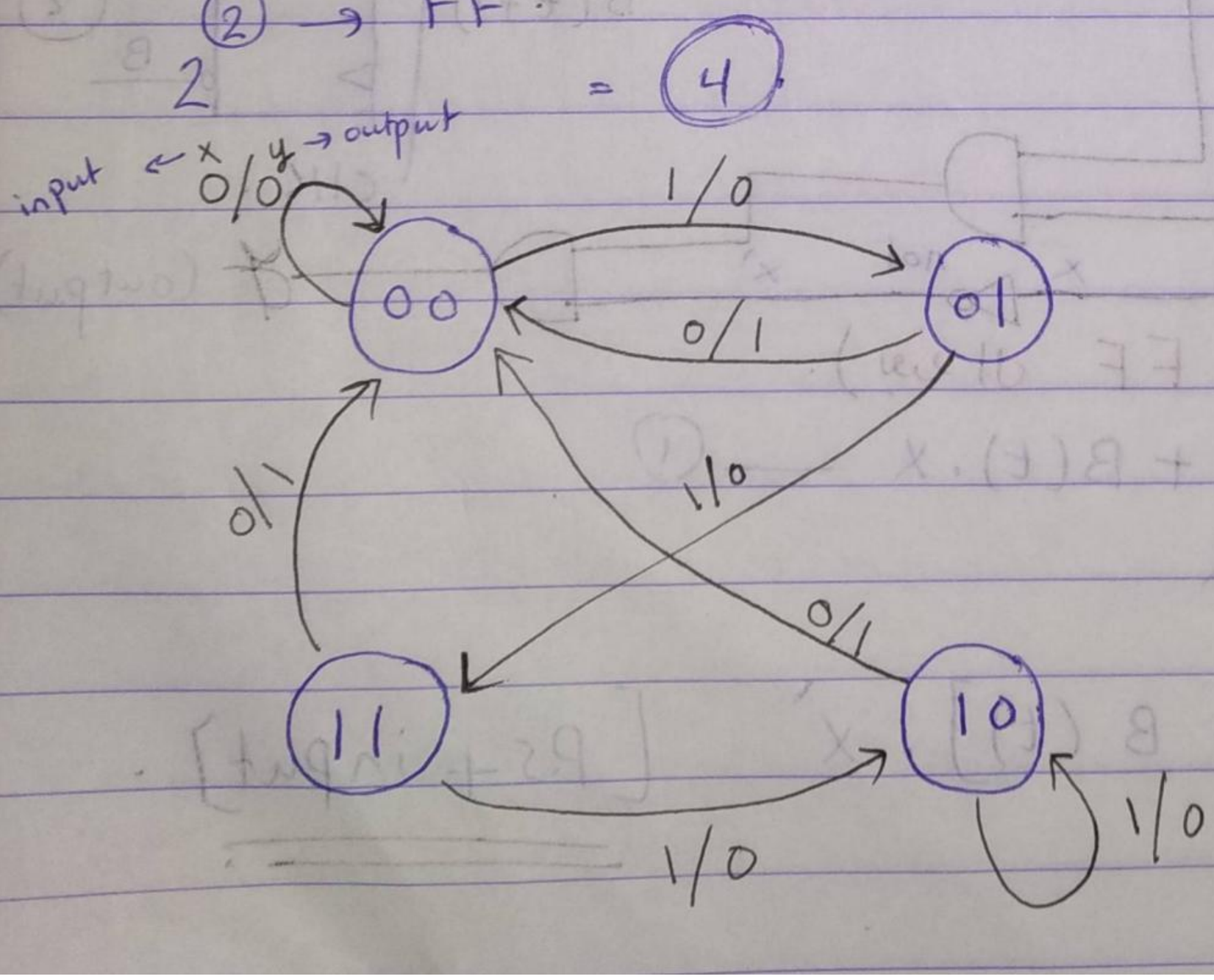
$B(t+1) = \bar{A}(t).X$

$y = [A(t) + B(t)].\bar{x}$

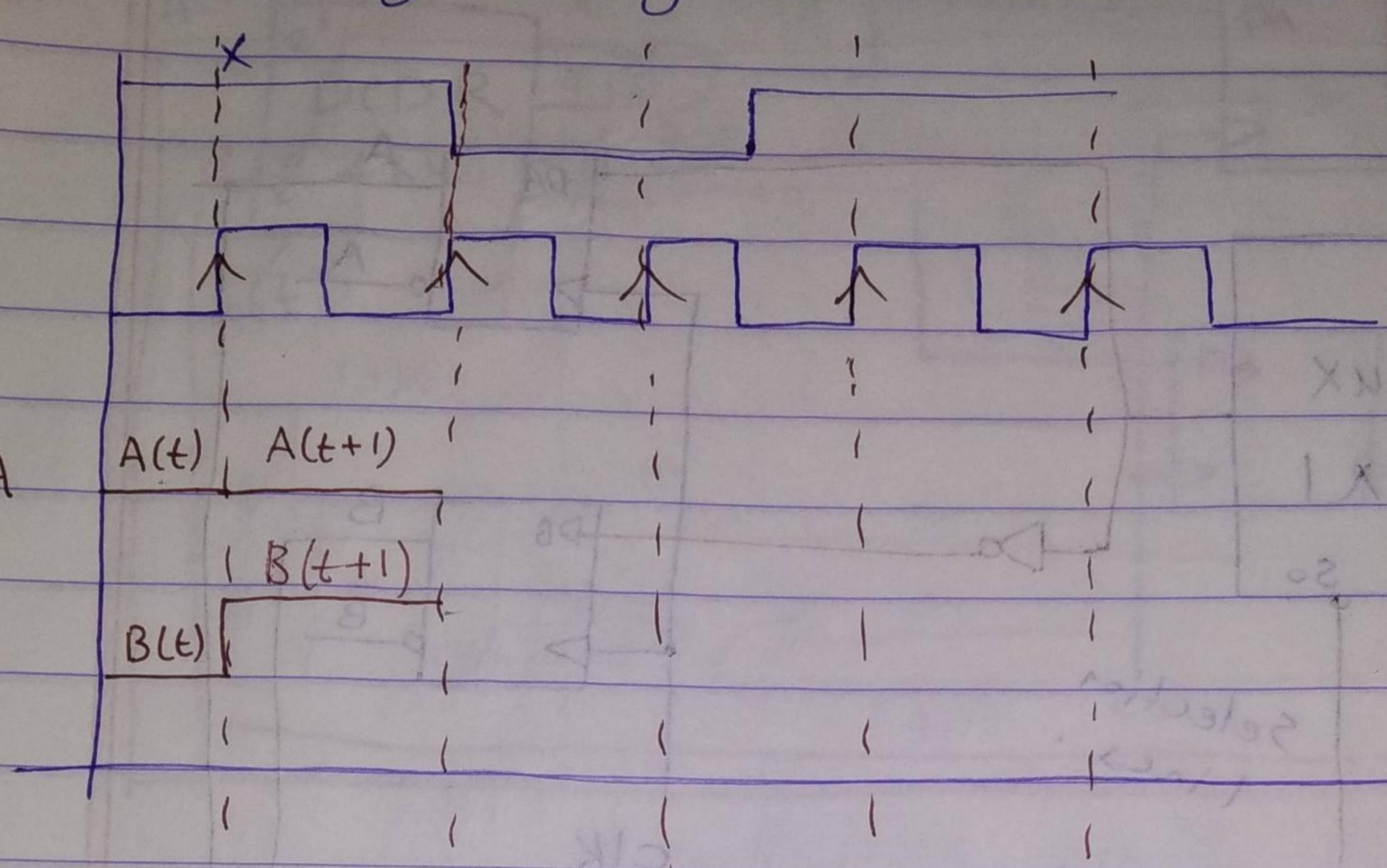
③ State Diagram

② → FF

$2^2 = 4$



(4) Timing Diagram.



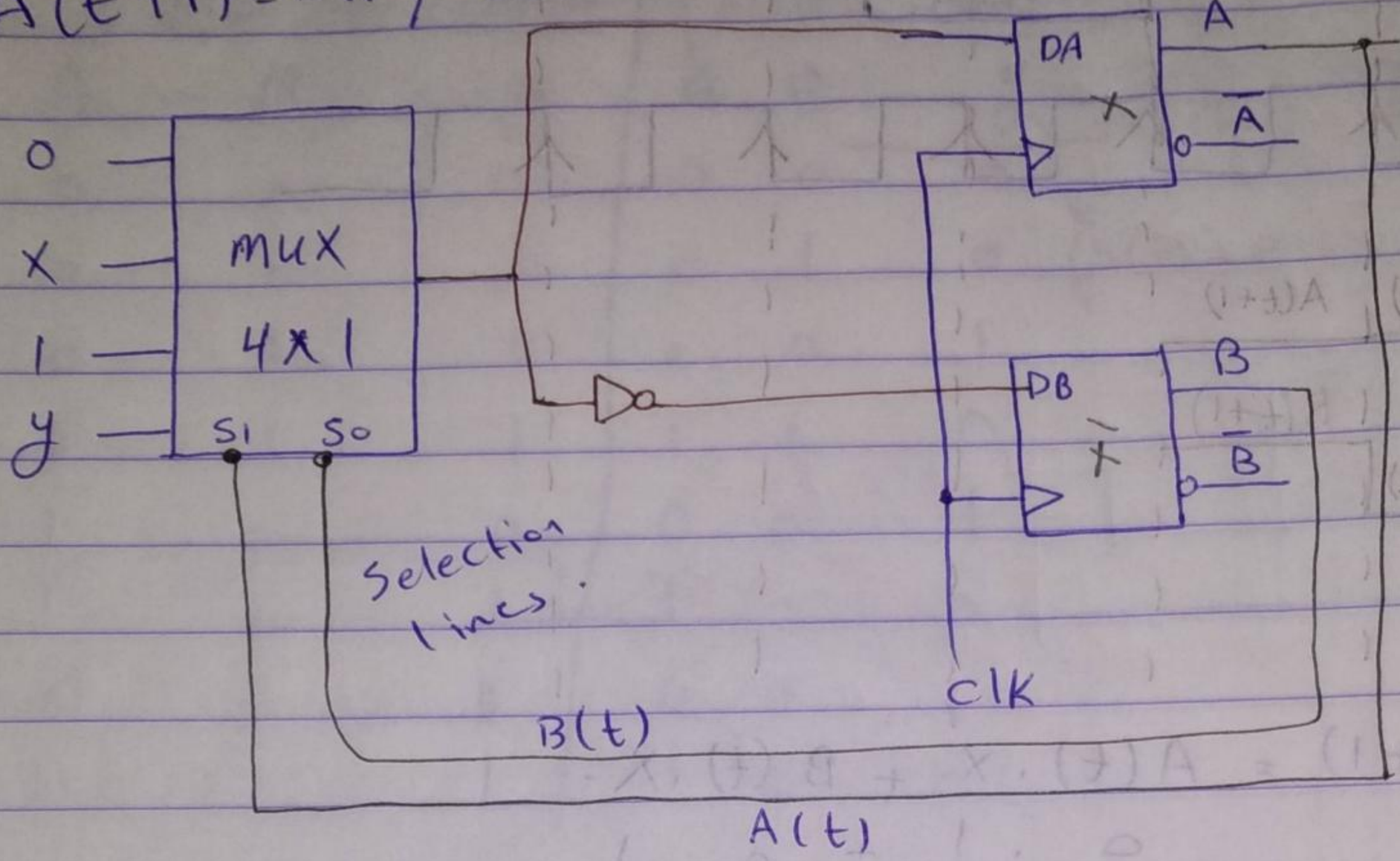
$$A(t+1) = A(t).X + B(t).X.$$
$$0 \quad .1 + 0 \quad .1$$

$$B(t+1) = \bar{A}(t).X$$
$$\bar{0} \quad .1$$

بنكملها

ex

$A(t+1) = DA$ / $B(t+1) = D_B$.

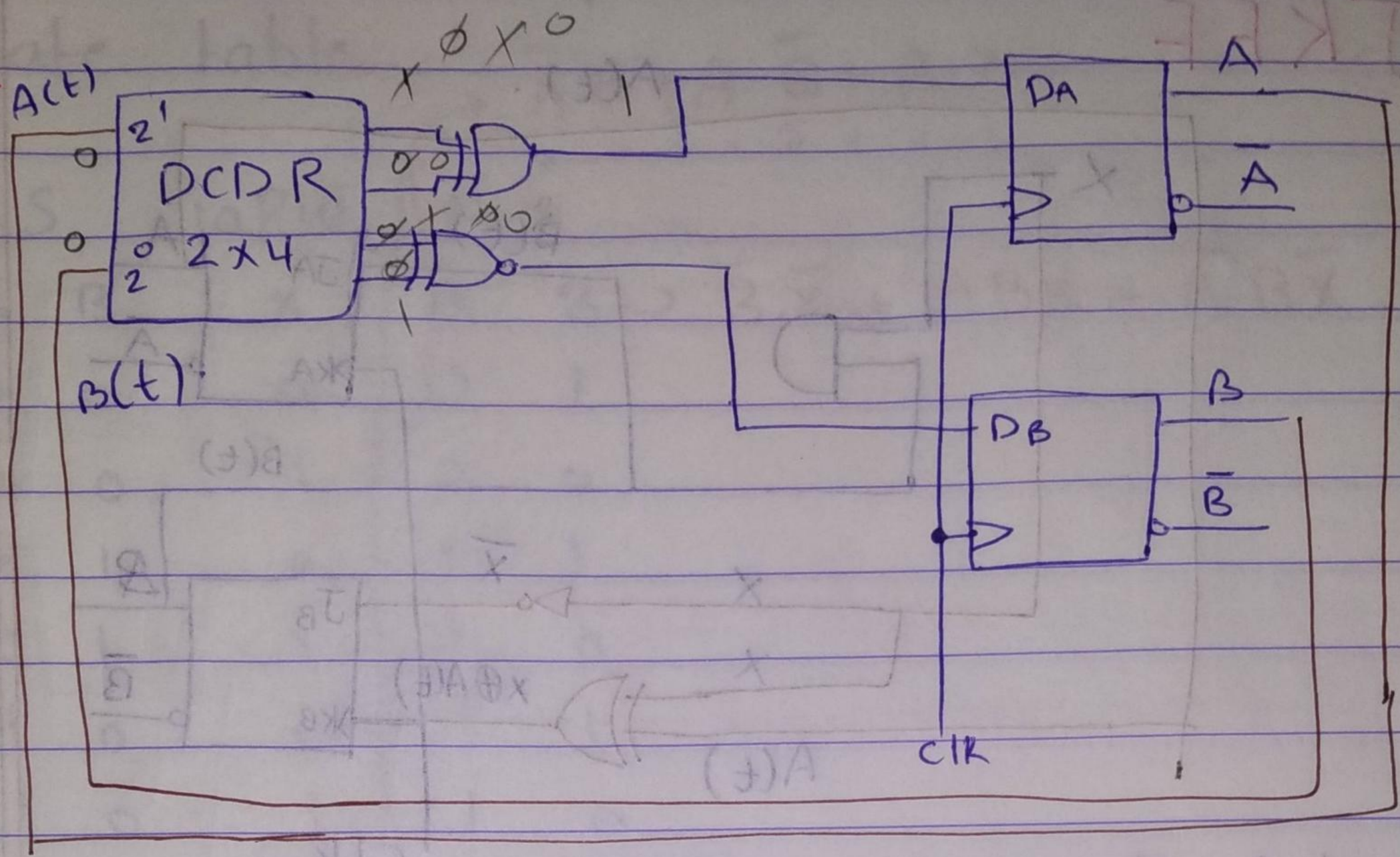


P.S		input		N.S	
A	B	x	y	A	B
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	1	1
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	0	0
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	1	1	0

$\tilde{x}$

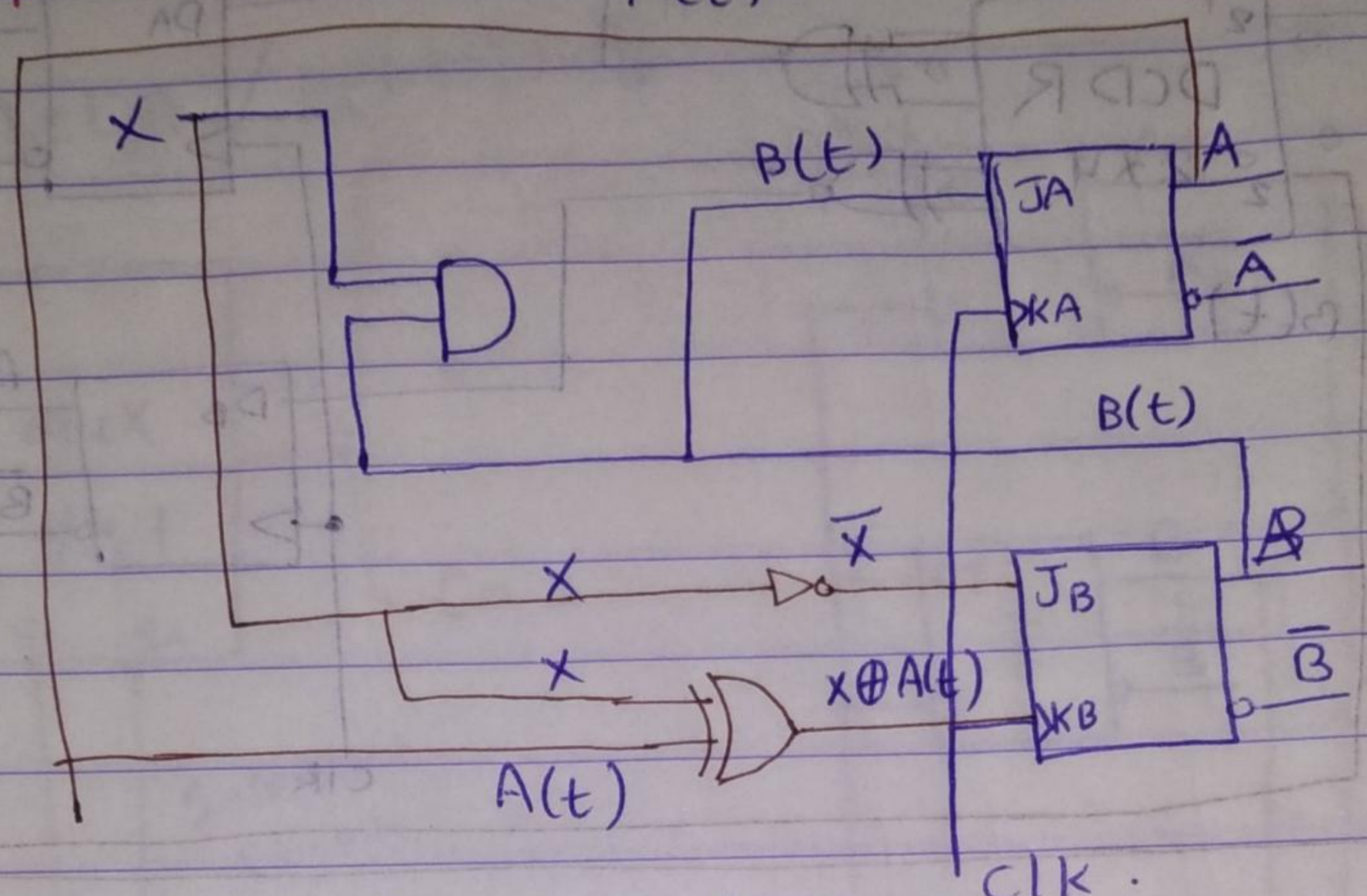
	00	01	11	10
00				
01			1	1
11				
10				

ex



P.S		N.S	
A	B	A	B
0	0	1	1
0	1	1	0
1	0	0	0
1	1	0	0

JKFF



- what is the State equation

Two State eqn ..

$$A(t+1) = J_A \bar{A}(t) + \bar{K} A A(t).$$

$$= B(t) \cdot \bar{A}(t) + [x \cdot B(t)] \cdot A(t).$$

$$A(t+1) = A'B + A\bar{B} + A.x \quad \text{—— (1)}$$

$$B(t+1) = J_B . \bar{B}(t) + \bar{K}_B B(t).$$

$$= \bar{x} \cdot \bar{B}(t) + (x \oplus A(t+1))' B(t).$$

$$= \bar{X} \cdot \bar{B}(t) + [\bar{x} \cdot A + x\bar{A}]' B(t).$$

$$= \bar{B}\bar{x} + ABX + \bar{A}B\bar{X}. \quad \text{— (2)}.$$

② State table.

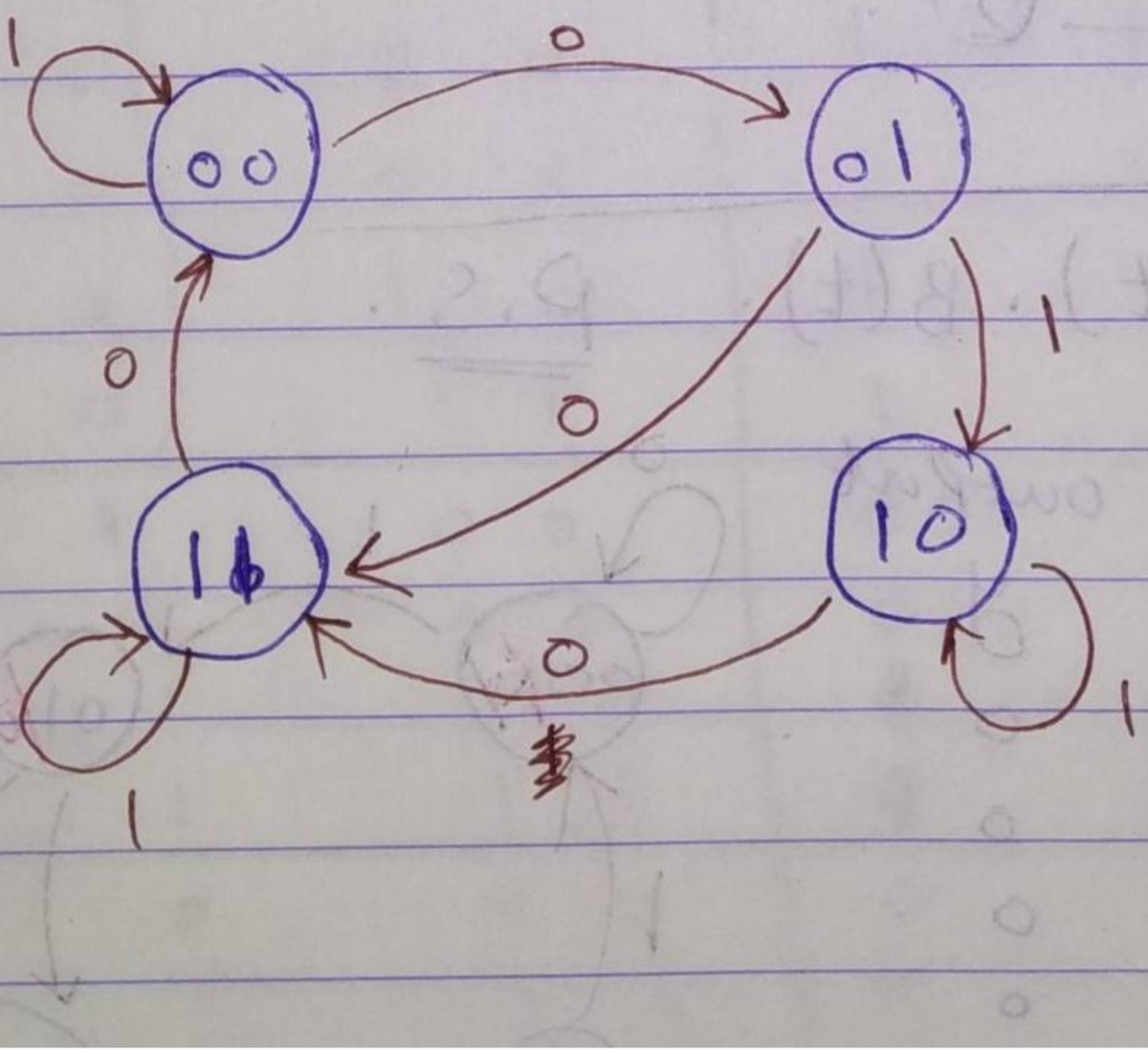
$\bar{A}.B + A.\bar{B} + A.X$.

$\bar{0}.0 + 0.\bar{0} + 0.1$

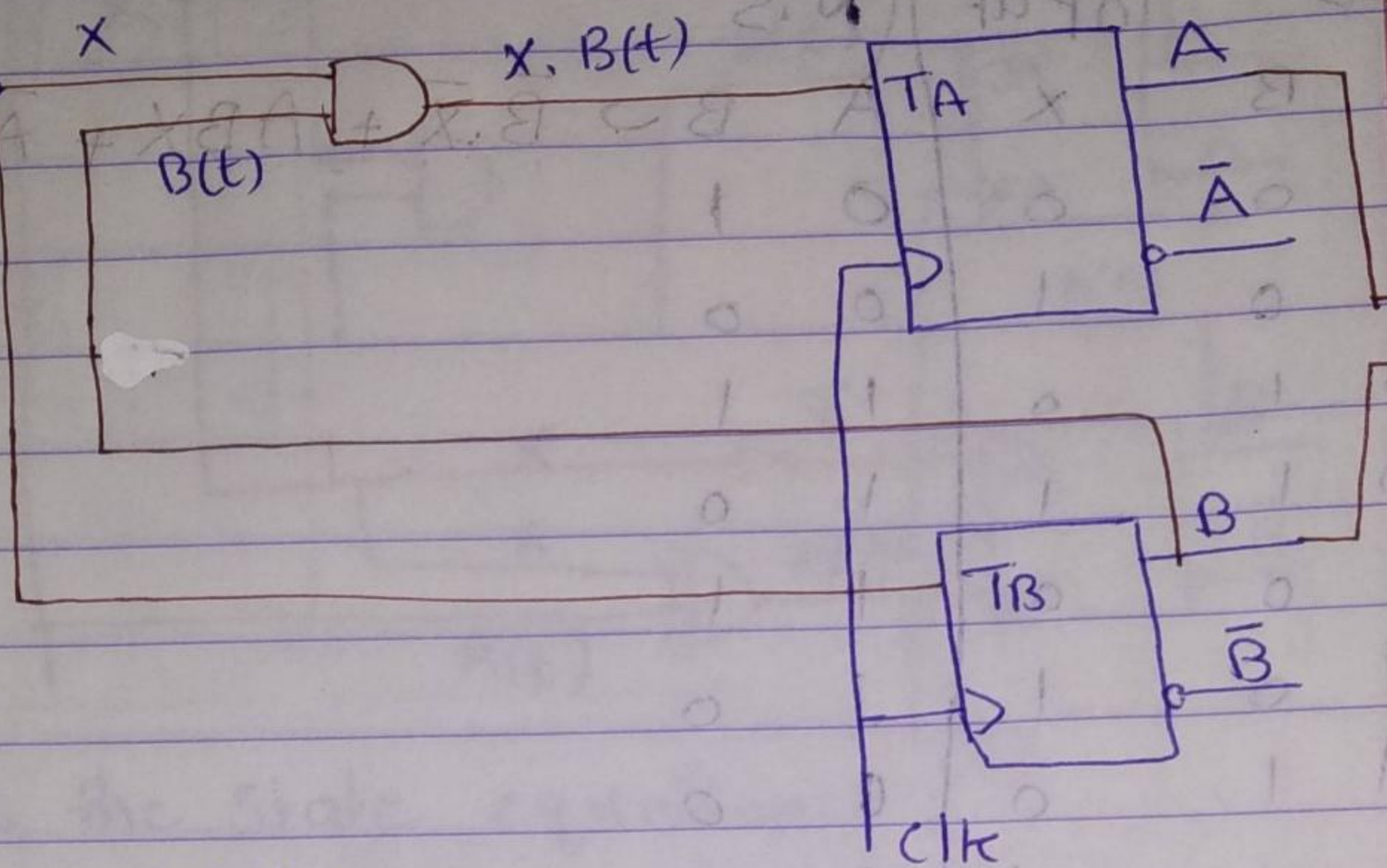
P.S		input	N.S	
A	B	X	A	B
0	0	0	0	1
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

$B \rightarrow \bar{B}.\bar{X} + ABX + \bar{A}B\bar{X}$.

③ State Diagram.



ex



$A(t+1) = T_A \oplus A(t)$.

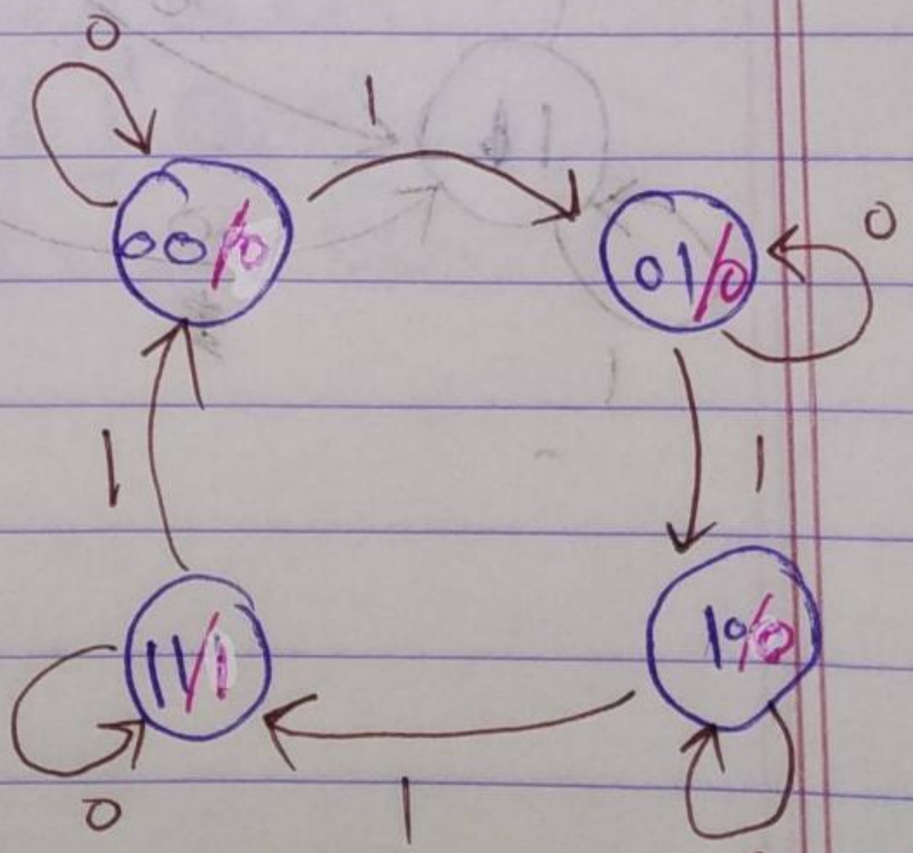
$A(t+1) = [X.B] \oplus A$ —— ①

$B(t+1) = T_B \oplus B(t)$.

$= X \oplus B$ —— ② .

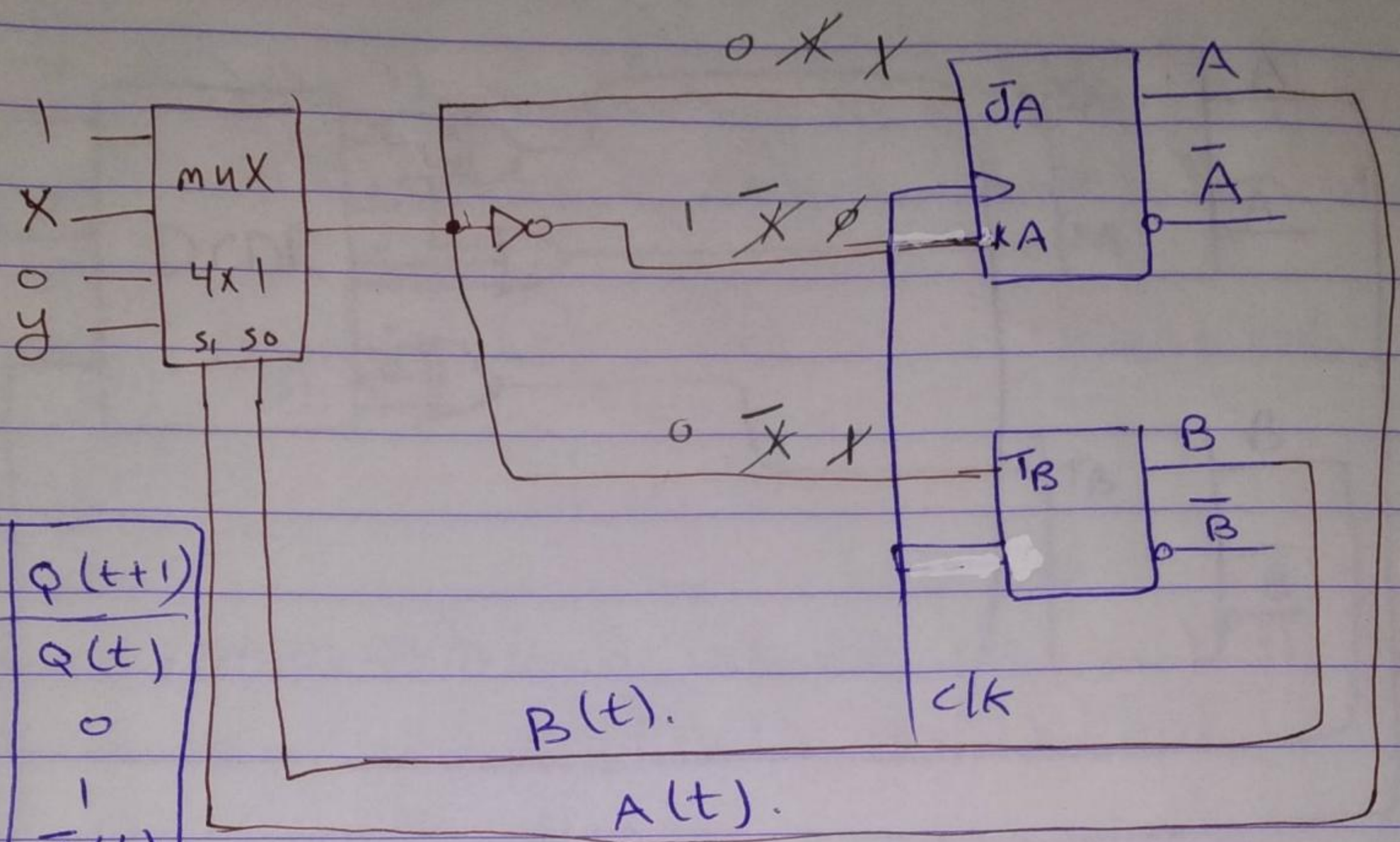
output $y = A(t) \cdot B(t)$. P.S.

P.S		input	N.S		output
A	B	X	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1



هنا ال output داخل الدوائر لأنه يعتمد على P.S فقط.

ex

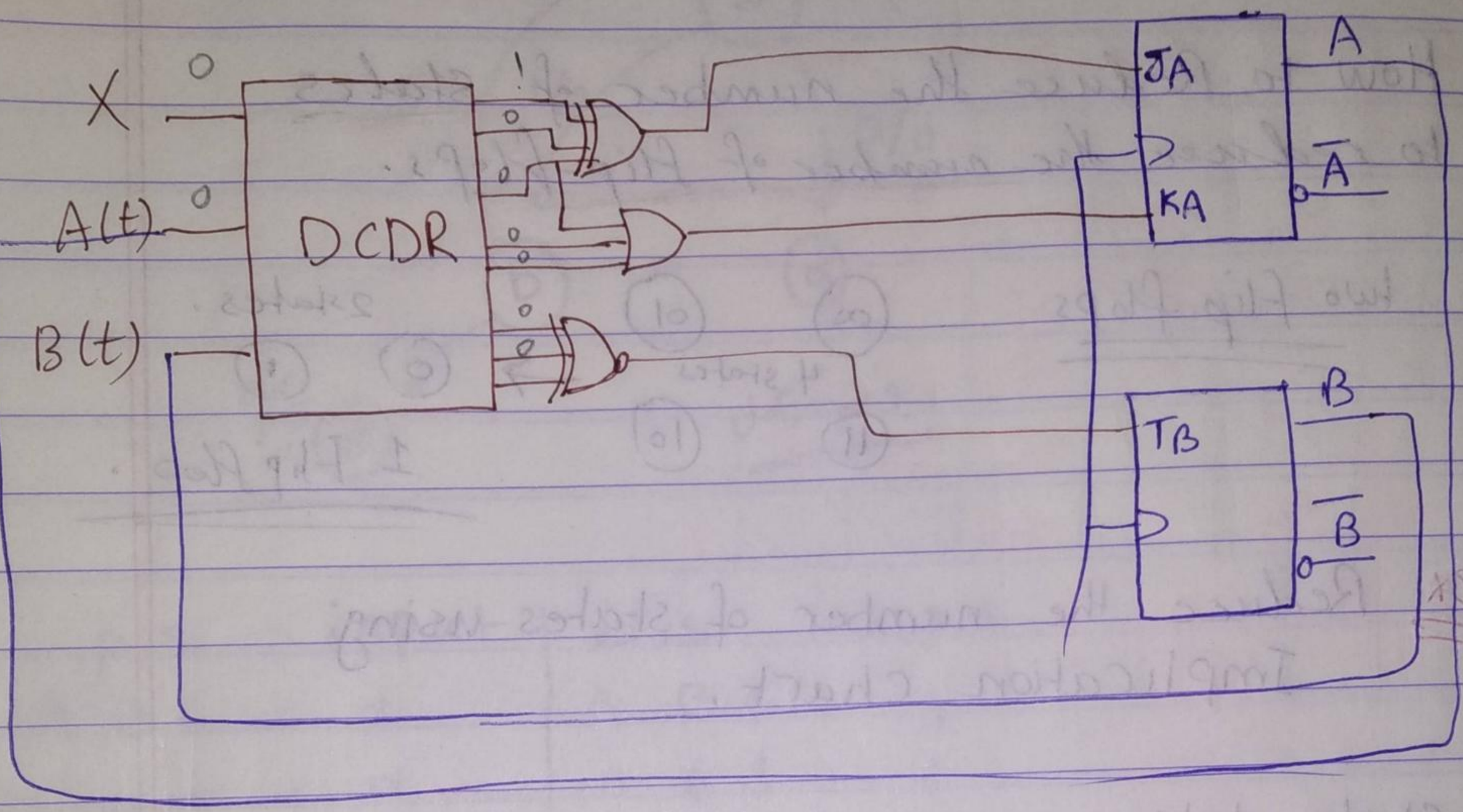


J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\bar{Q}(t)$

T	Q(t+1)
0	Q(t)
1	$\bar{Q}(t)$

P.S		input		N.S	
S_1 A	B S_0	x	y	A	B
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	1	0
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	0	1

مش متأكدة منه.
(اذا غلط اكولي ٨_٨).



input	P.S		N.S	
X	A	B	A	B
0	0	0	1	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	0
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q}$(t).

T	Q(t+1)
0	Q(t)
1	$\overline{Q}$(t).

طريقة الاختزال.

Implication chart for State Reduction.

How to Reduce the number of states
to reduce the number of flip-flops.

two flip-flops → (00) (01) (11) (10) 4 states

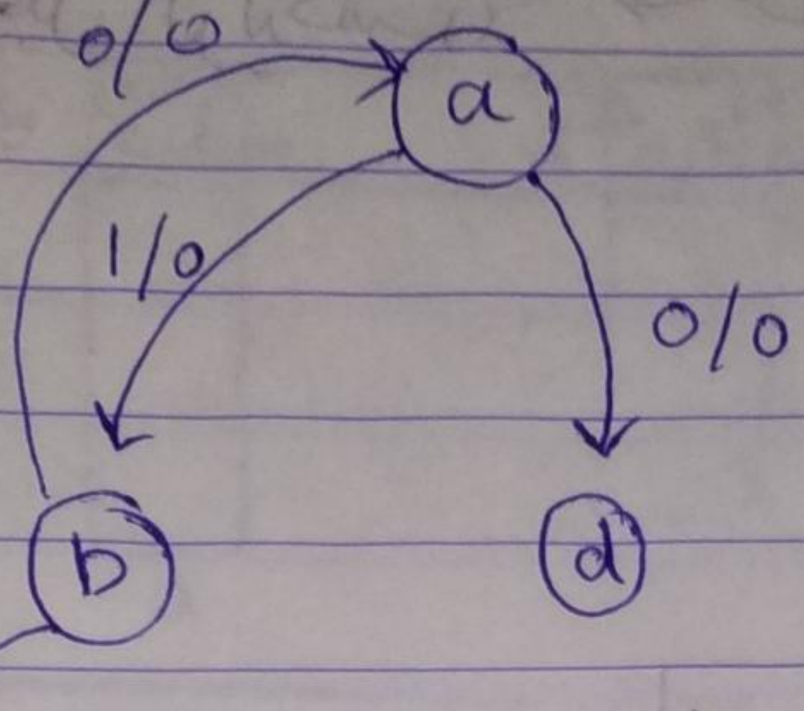
→ (0) (1) 2 states.

→ 1 flip flop.

Reduce the number of states using Implication chart.

State table

P.S	N.S x=0	N.S x=1	output x=0	output x=1
000 a	d	b	0	0
001 b	e	a	0	0
010 c	g	f	0	1
011 d	a	d	1	0
100 e	a	d	1	0
101 f	c	b	0	0
110 g	a	e	1	0
111 -	-	-	-	-



وبتكمل.

P.S input				N.S output.			
A	B	C	x	A	B	C	y
0	0	0	0	0	0	1	0
0	0	0	1	0	0	1	0
0	0	1	0	1	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0				
1	1	1	1				

7 flip flops ⟿ قبل الريدكشن

b	d,e ~~a,b~~ ✓					
c	X	X				
d	X	X	X			
e	X	X	X	✓		
f	c,d ~~b,b~~ X	c,e a,b X	X	X	X	
g	X	X	X	~~a,a~~ d,e ✓	~~a,a~~ d,e ✓	X
	a	b	c	d	e	f

① بنحط X اذا كانوا ال two state بيعطوا different output

② two state ⇒ same output & same next state. (✓)

(a,b), (d,e), (d,g), (e,g) equivalent

(a,b) (d,e,g) ↵

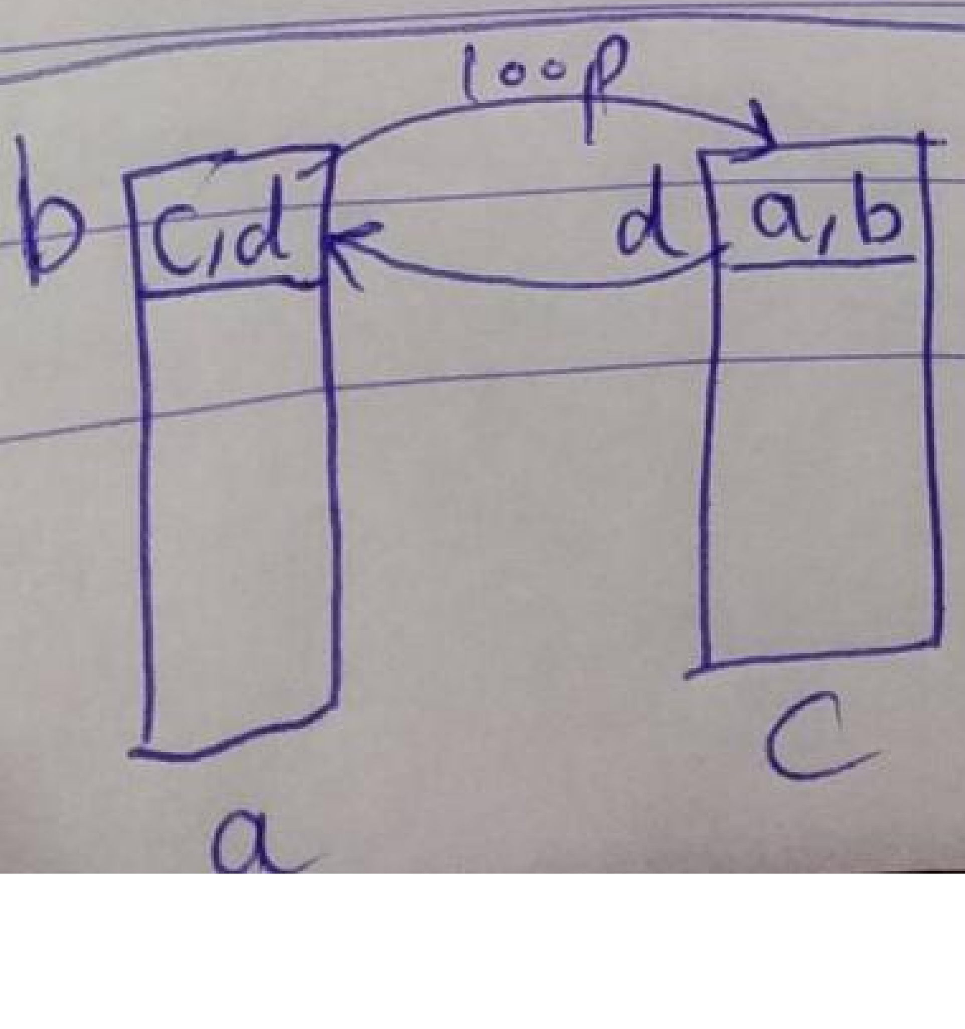
a ≡ b

d ≡ e ≡ g.

p.s	N.S	output
a	d a	0 0
c	d f	0 1
d	a d	1 0
f	c a	0 0

4 state بدل 7

loop

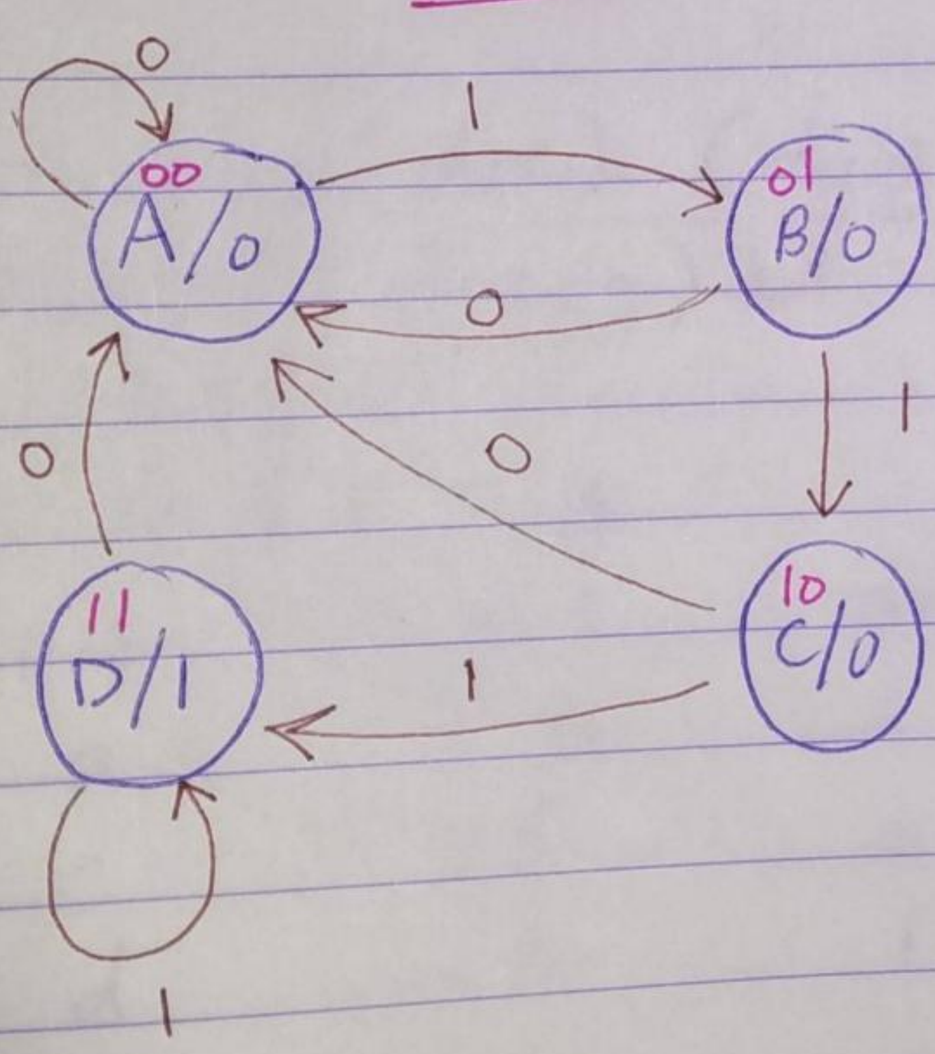


* Design procedure. المراحل

① Read the problem carefully
② Derive the state Diagram.
③ Assign Binary values to the states.
④ State Table.
⑤ Determine the type of flip flop.
⑥ Derive the input equation.
⑦ Draw the circit.

ex Design asequential cercit that deticts three or more consecutive one's? (DFF)

111 1011
x



p.s		input	N.S		output
			DA	DB	
A	B	X	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

ال output يعتمد فقط على ال p.s

, more أو 00/0 01/0 10/0 11/1

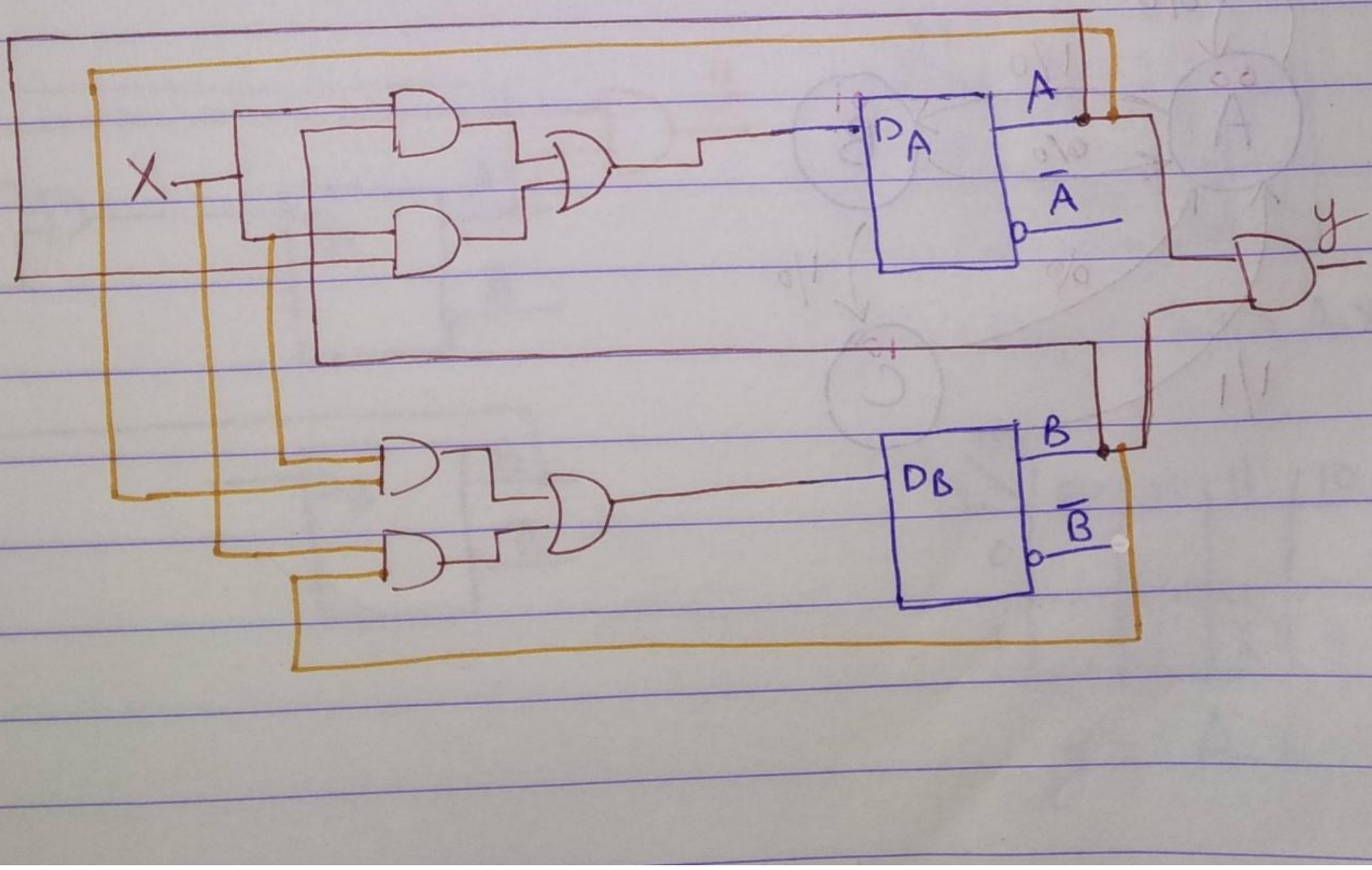
B(t) X / A(t)	00	01	11	10
0			1	
1		1	1	

$D(A) = A(t+1)$

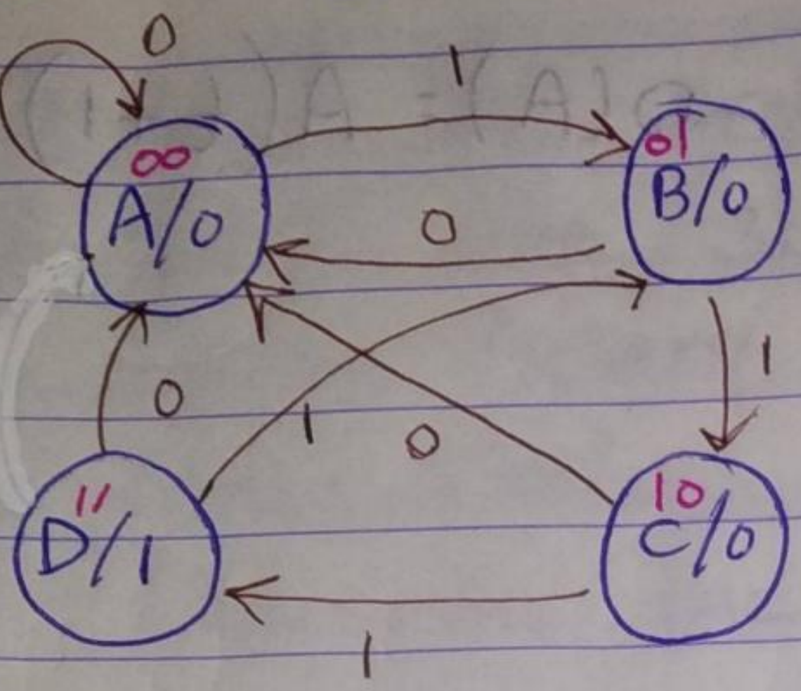
$DA = B.X + A.X$

BX / A	00	01	11	10
0		1		
1		1	1	

$B(t+1) = DB = \bar{B}X + AX$



ex Design to detect three Consecutive ones ?

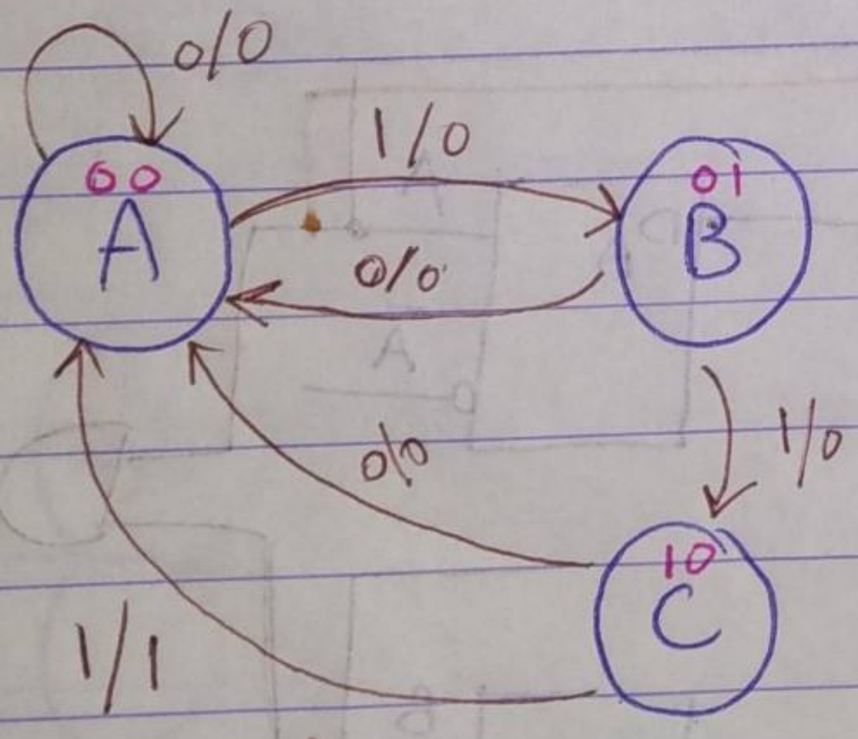


111 111

1 1

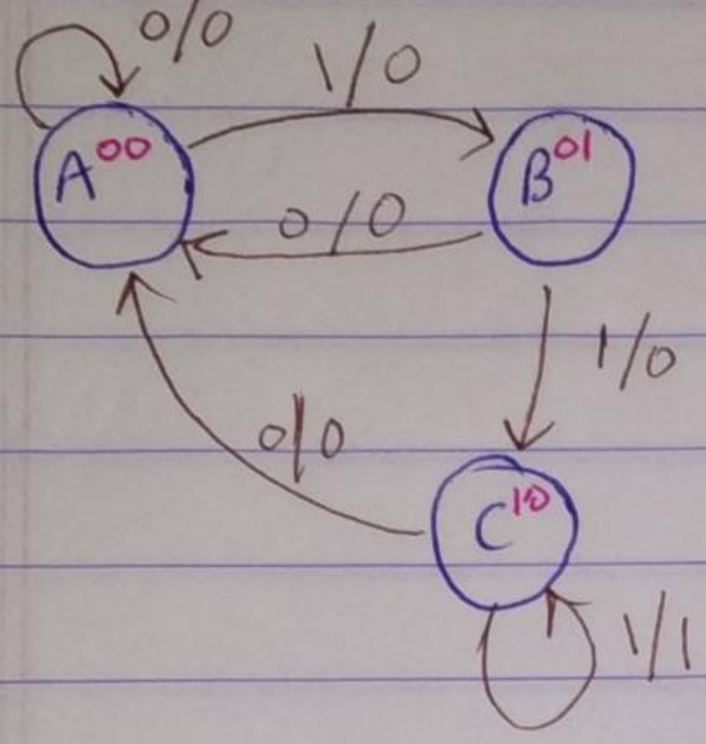
P.S	input	N.S	output
A B	x	A B	y
0 0	0	0 0	0
	1	0 1	0
0 1	0	0 0	0
	1	1 0	0
1 0	0	0 0	0
	1	1 1	0
1 1	0	0 0	1
	1	0 0	1

ex Design a circit to detect 3 Consecutive ones ? Mealy



ex Design synchronous sequential circit to detect three or more consecutive ones?

mealy



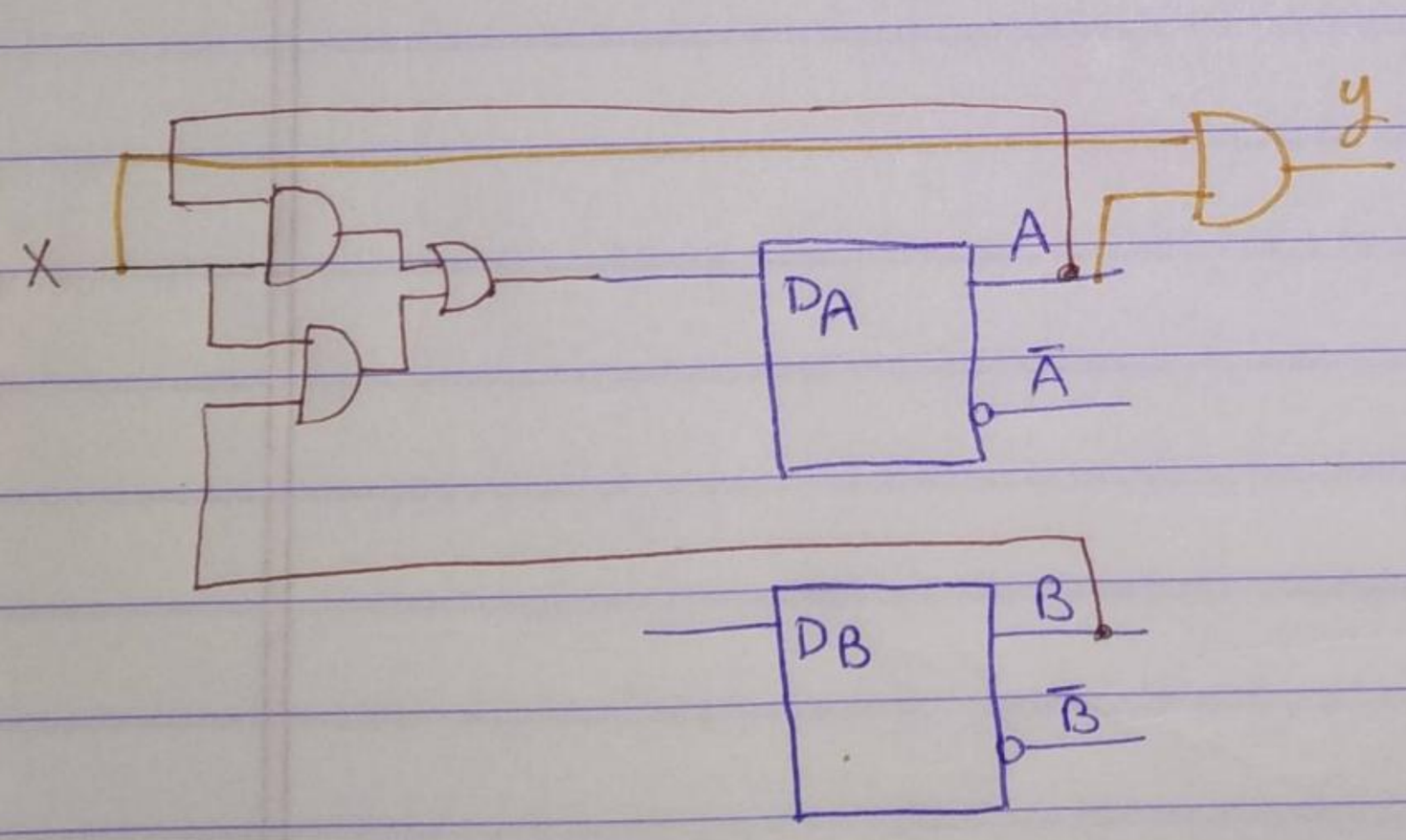
P.S		input	N.S		output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	0	1
1	1	0	x	x	x
1	1	1	x	x	x

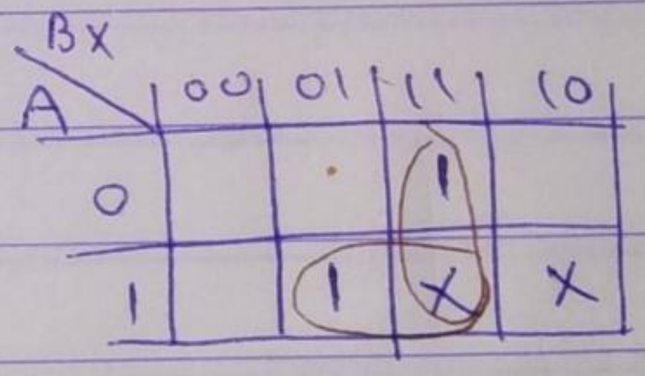
حالات موجودة.

D-ff.

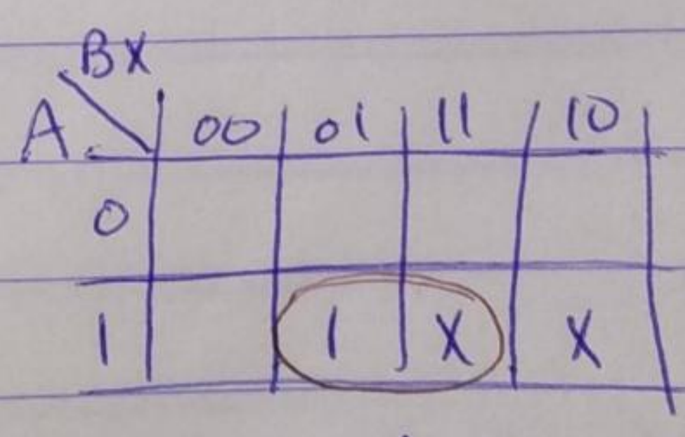
$A(t+1) = D_A$.

$B(t+1) = D_B$.





$D_A = B.X + A.X$.



$y = A.X$

ex Design synchronous circit to detect three or more ones? Consecutive فقط